Electronic Devices and Circuits

Laboratory Manual

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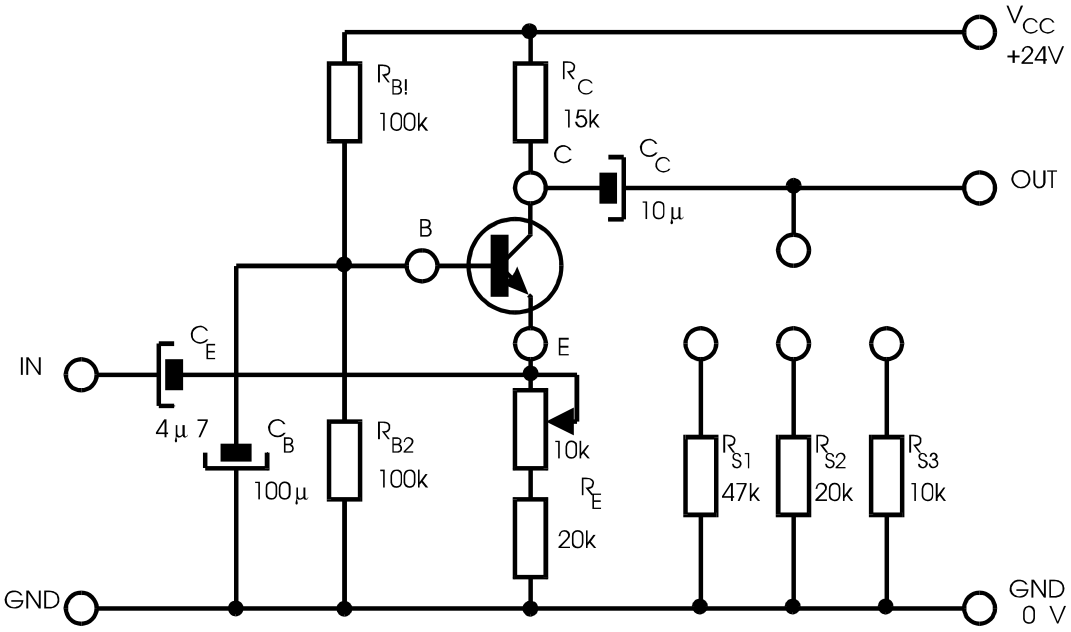
1. Bipolar Junction Transistor Amplifier Circuit, in Common Base Configuration

Introduction

The amplifier circuit in the laboratory contains a bipolar junction transistor in common base configuration. The circuit is powered from a single power supply, and the transistor is biased through a resistive divider in the base:



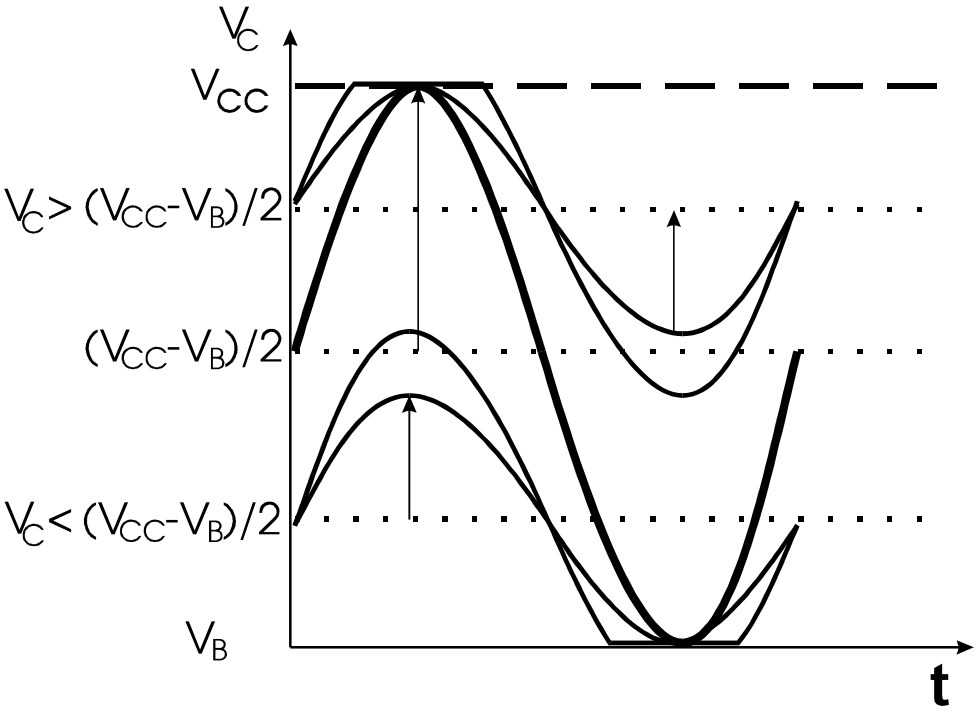
The R_E resistor is made out of a fixed resistor in series with a potentiometer, allowing for the adjustment of the quiescence emitter current for proper operation.

At the output of the circuit, three load resistors R_{S1}, R_{S2}, R_{S3} can be connected. For different load resistors, the parameters of the AC operation (e.g. voltage amplification) will be affected, but not the static operating point.

Experiment

a. Setting the static operating point.

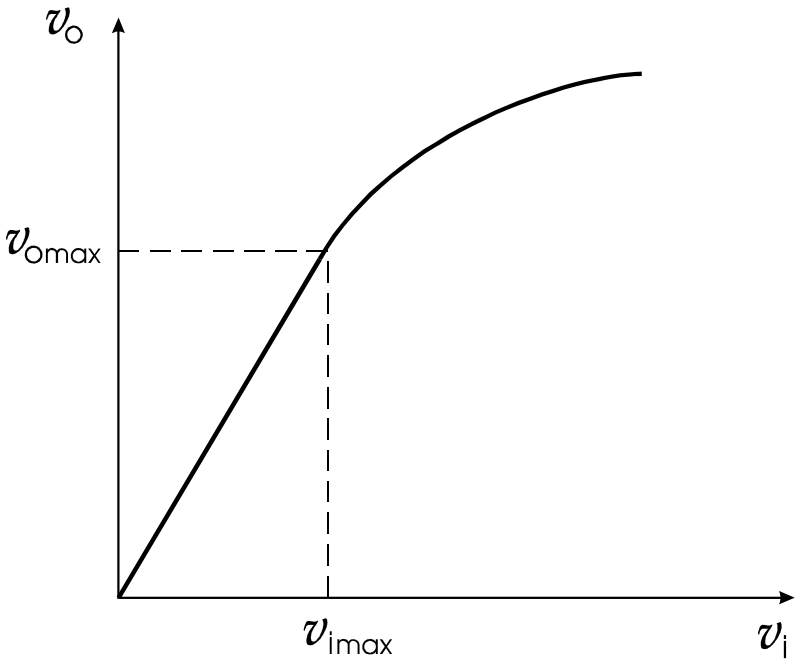
1. The circuit is powered by a +24V DC power supply connected to the banana jacks labeled VCC (+24V) and GND.
2. Using a DC voltmeter, the voltages V_E, V_B and V_C have to be measured at the E, B şi C test points (banana jacks), using ground as reference. While adjusting the potentiometer in the emitter, please observe the variations in any of the three voltages. You will note that the base and emitter voltages are little affected by the potentiometer adjustments.



3. In order to bias the transistor in order to obtain a maximal voltage swing at the output, as shown in the figure above, the voltage difference between the collector and base has to be set to half the voltage difference U_1 between the supply voltage (V_{CC}=+24V) and base (V_B). Calculate $U_1=V_{CC}-V_B$ and half of this value, $U_2=U_1/2$. The collector voltage will have to be $V_C=V_B+U_2$ (same as $V_C=V_{CC}-U_2$).
4. Set the V_C to the value calculated above by adjusting the potentiometer in the emitter.

b. Input-output transfer characteristic v_o=f(v_i).

5. Connect at the amplifier input (between IN şi GND banana jacks) a signal generator. Set the signal frequency to about 1000 Hz. As the input impedance for the common base configuration is very small, due to finite output resistance of the generator, the actual input voltage will be different from the set value. Connect therefore an additional AC voltmeter at the input to read the actual input signal. Leave all of the R_{s1},R_{s2} and R_{s3} unconnected. As a result, the load resistor will be R_c.
6. Adjust the signal generator output such that the input voltage v_i varies in the range 10 mV – 100 mV and measure the output voltage v_o. Take about 10 points and plot v_o=f(v_i). Please note the linear region and the saturation region.
7. Connect an oscilloscope at the output to visualize the signal waveforms in the linear region and saturation region of the transfer characteristic.

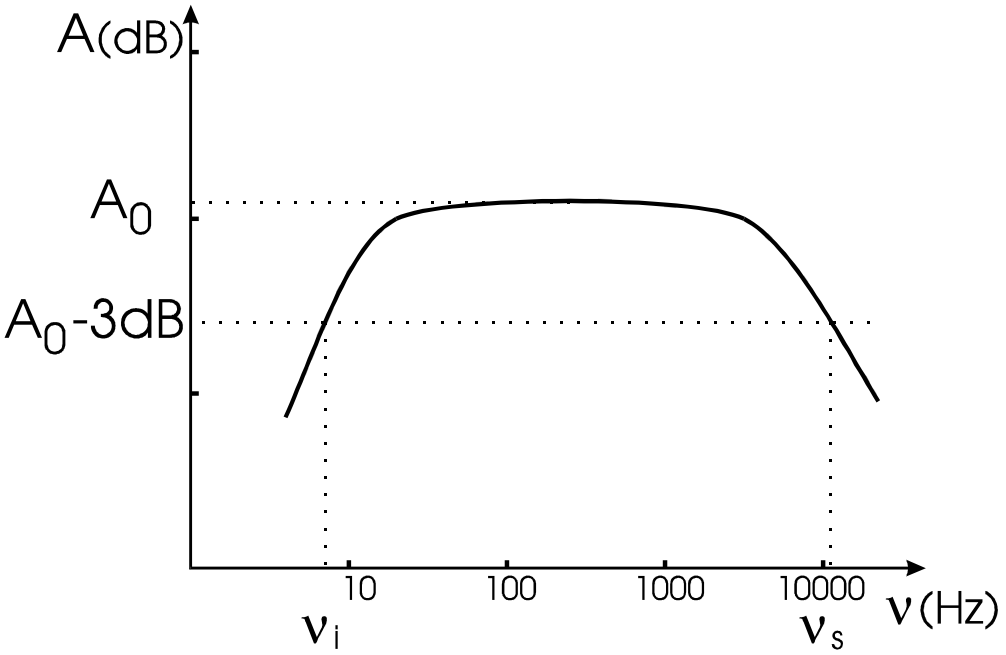


8. Connect the load resistor R_{s1} at the output. As a result, the equivalent output load resistance will be R_{s1} in parallel with R_c. Repeat steps 6-7 and plot the transfer characteristics on the same figure. Cycle through resistors R_{s2} and R_{s3}.
9. Check whether the equivalent load resistance $R_c||R_{sk}$ (k=1-3) is proportional to $A=v_o/v_i$ in the linear region.

c. Frequency characteristic A=f(ν).

10. Select an input voltage within the linear region for no load resistor connected at the output.
11. While maintaining the input voltage constant, select a set of different frequencies in the 1 Hz - 10 MHz range. Use a logarithmic frequency scale, i.e. 1, 2, 5, 10, 20, 50 Hz and so on.
12. At each frequency, write down the output voltage amplitude and calculate the voltage amplification:

$$A = \frac{V_o}{V_i}$$



13. Using the set of (ν,A) pairs that are obtained, plot the frequency characteristic A=f(ν) in a double logarithmic scale, i.e. log(A)=f(log(ν)). The voltage gain is 20log(A) and is measured in decibels (dB).
14. Repeat the steps 11-13 for all load resistors. Plot the curves on the same figure.
15. Calculate the high-cutoff (ν_s) and low-cutoff (ν_i) frequencies at which the amplification drops to $\frac{1}{\sqrt{2}}$ of its maximum value A_0, $A = A_0/\sqrt{2}$. In terms of voltage gain, that corresponds to a 3 dB decrease.
16. Calculate the frequency band B for each load resistor:

$$B = \nu_s - \nu_i$$

18. Calculate the amplification – frequency band product, A·B, for no load and for each different load resistor.

19. Please write down the values calculated at steps 15-18 in the table below:

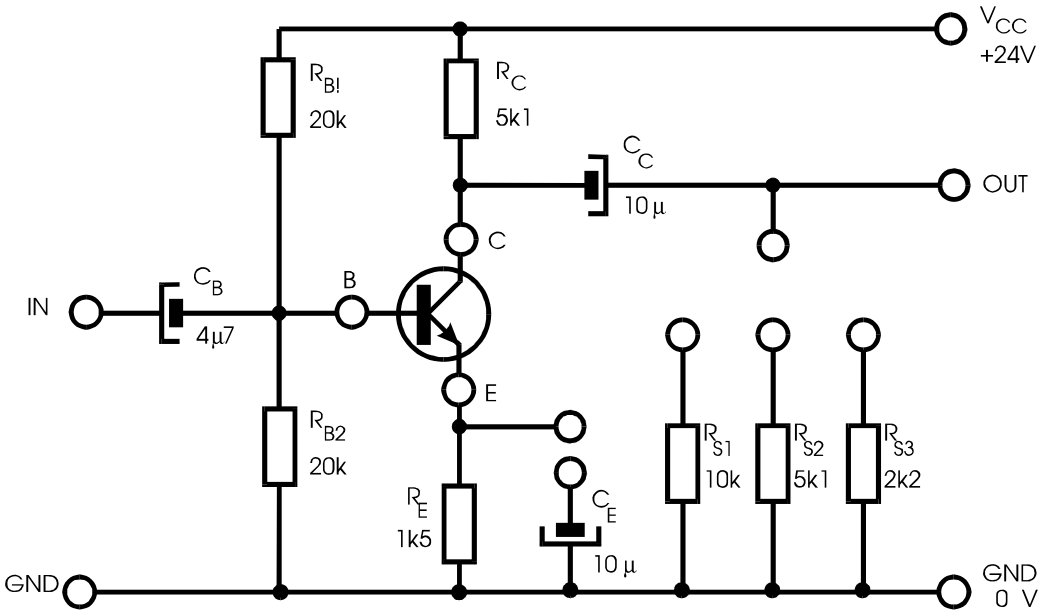
Rs	A=vo/vi	νi	νs	B=νs-νi	A·B
-					
Rs1					
Rs2					
Rs3					

Check that the amplification - frequency band product is nearly constant, regardless of the load resistor and associated voltage amplification factor.

2. Bipolar Junction Transistor Amplifier Circuit, in Common Emitter Configuration

Introduction

The amplifier circuit in the laboratory contains a bipolar junction transistor in common emitter configuration. The circuit is powered from a single power supply, and the transistor is biased through a resistive divider in the base:

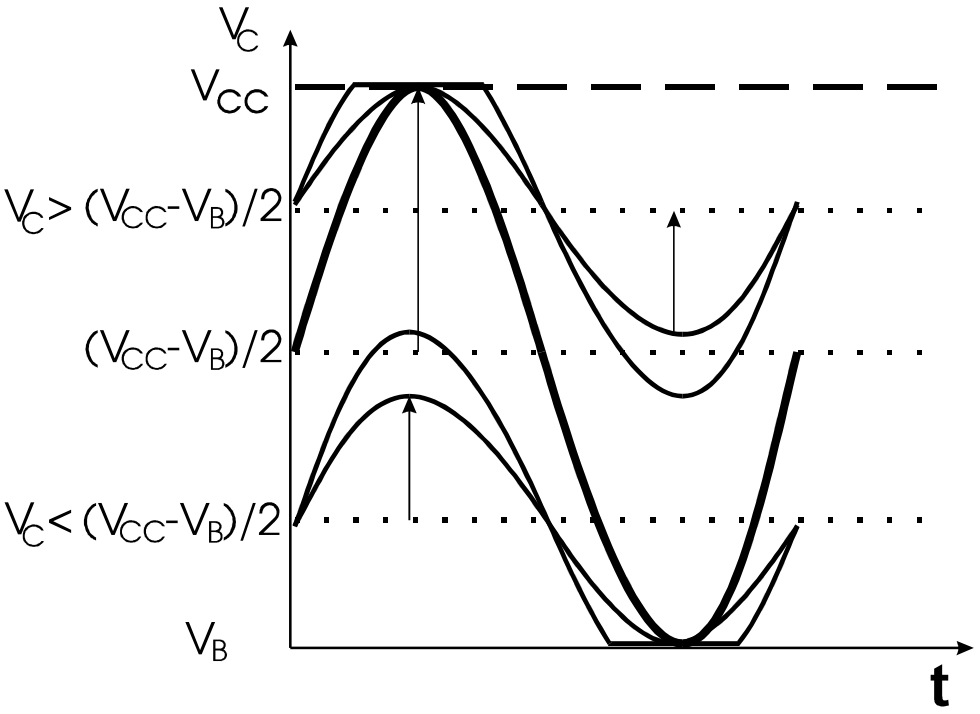


In parallel with the R_E resistor that allows shunting the resistor in AC.
At the output of the circuit, three load resistors R_{S1}, R_{S2}, R_{S3} can be connected. For different load resistors, the parameters of the AC operation (e.g. voltage amplification) will be affected, but not the static operating point.

Experiment

a. Checking the static operating point.

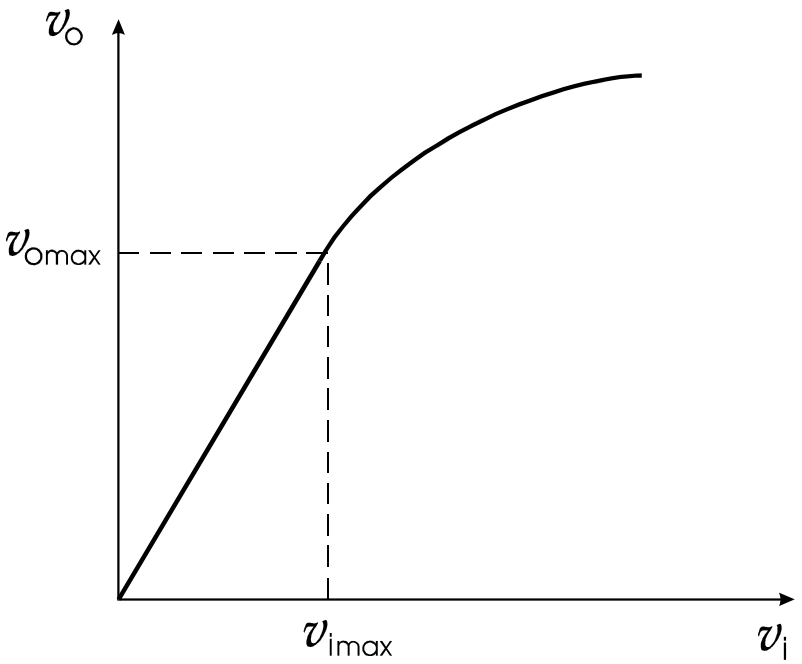
1. The circuit is powered from a +24V DC power supply connected to the banana jacks labeled VCC (+24V) and GND.
2. Using a DC voltmeter, the voltages V_E, V_B and V_C have to be measured at the E, B şi C test points (banana jacks), using ground as reference.



3. In order to bias the transistor in order to obtain a maximal voltage swing at the output, as shown in the figure above, the voltage difference between the collector and base has to be about half the voltage difference U_1 between the supply voltage (V_{CC}=+24V) and base (V_B). Calculate $U_1=V_{CC}-V_B$ and half of this value, $U_2=U_1/2$. Check that the collector voltage value is close to $V_C=V_B+U_2$ (same as $V_C=V_{CC}-U_2$).

b. Input-output transfer characteristic v_o**=f(**v_i**).**

5. Make sure that the capacitor C_E in parallel with R_E is disconnected. Connect at the amplifier input (between IN şi GND banana jacks) a signal generator. Set the signal frequency to about 1000 Hz. As the input impedance for the common base configuration is very small, due to finite output resistance of the generator, the actual input voltage will be different from the set value. Connect therefore an additional AC voltmeter at the input to read the actual input signal. Leave all of the R_{s1},R_{s2} and R_{s3} unconnected. As a result, the load resistor will be R_c.
6. Adjust the signal generator output such that the input voltage v_i varies in the range 50 mV – 500 mV and measure the output voltage v_o. Take about 10 points and plot v_o**=f(**v_i**).** Please note the linear region and the saturation region.
7. Connect an oscilloscope at the output to visualize the signal waveforms in the linear region and saturation region of the transfer characteristic.

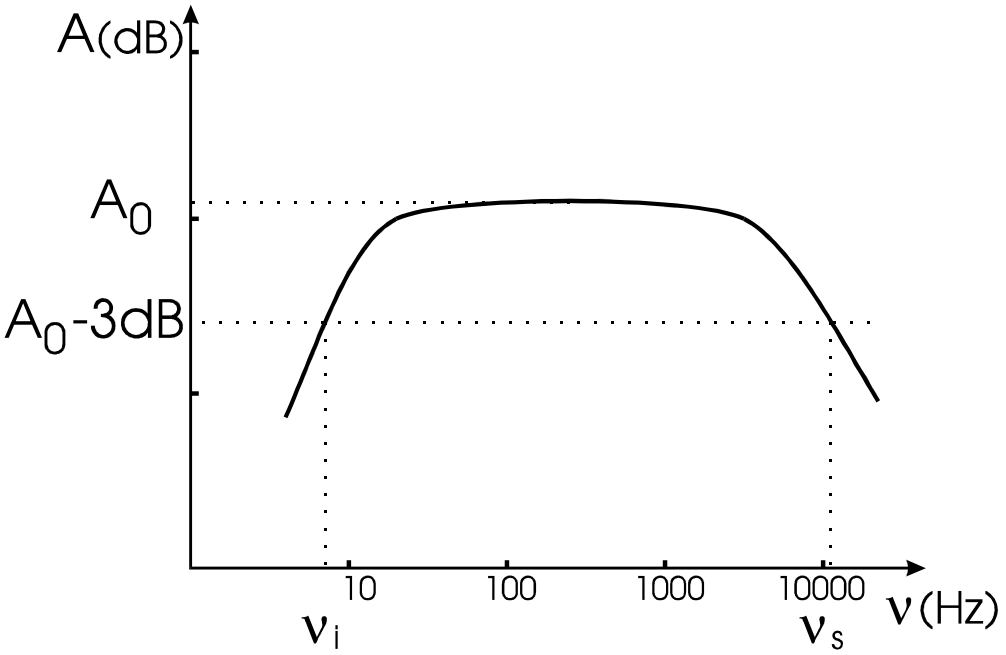


8. Connect the load resistor R_{s1} at the output. As a result, the equivalent output load resistance will be R_{s1} in parallel with R_c. Repeat steps 6-7 and plot the transfer characteristics on the same figure. Cycle through resistors R_{s2} and R_{s3}.
9. Check whether the equivalent load resistance $R_c||R_{sk}$ (k=1-3) is proportional to $A=v_o/v_i$ in the linear region.

c. Frequency characteristic A=f(ν).

10. Select an input voltage within the linear region for no load resistor connected at the output.
11. While maintaining the input voltage constant, select a set of different frequencies in the 1 Hz - 10 MHz range. Use a logarithmic frequency scale, i.e. 1, 2, 5, 10, 20, 50 Hz and so on.
12. At each frequency, write down the output voltage amplitude and calculate the voltage amplification:

$$A = \frac{\nu_o}{\nu_i}$$



13. Using the set of (ν,A) pairs that are obtained, plot the frequency characteristic A=f(ν) in a double logarithmic scale, i.e. log(A)=f(log(ν)). The voltage gain is 20log(A) and is measured in decibels (dB).
14. Repeat the steps 11-13 for all load resistors. Plot the curves on the same figure.
15. Calculate the high-cutoff (ν_s) and low-cutoff (ν_i) frequencies at which the amplification drops to $\frac{1}{\sqrt{2}}$ of its maximum value A_0, $A = A_0/\sqrt{2}$. In terms of voltage gain, that corresponds to a 3 dB decrease.
16. Calculate the frequency band B for each load resistor:

$$B = \nu_s - \nu_i$$

18. Calculate the amplification – frequency band product, A·B, for no load and for each different load resistor.

19. Please write down the values calculated at steps 15-18 in the table below:

Rs	A=vo/vi	νi	νs	B=νs-νi	A·B
-					
Rs1					
Rs2					
Rs3					

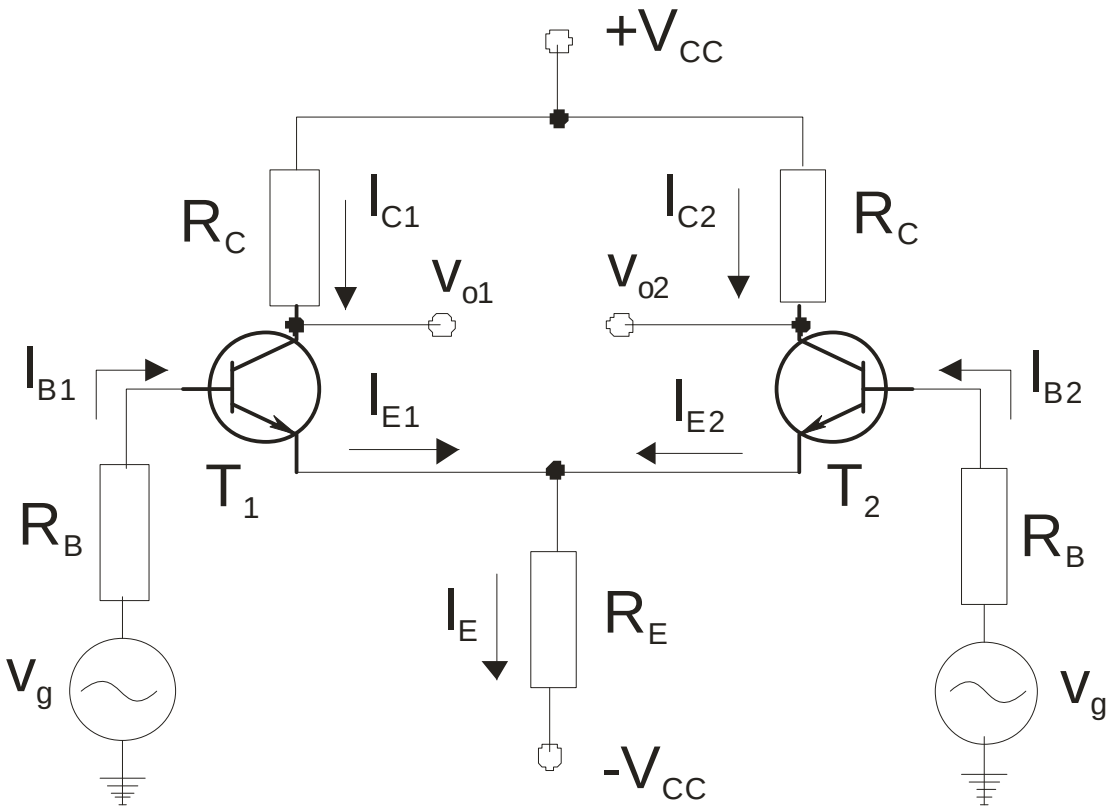
Check that the amplification - frequency band product is nearly constant, regardless of the load resistor and associated voltage amplification factor.

20. Connect the capacitor C_E in parallel with R_E and go again through steps 5 to 19, with the only difference that the input AC voltage values will have to be roughly 10 times lower than the ones previously used. As an example, for the transfer characteristic, the input voltage range will have to be 5 through 50 mV, in 5 mV steps. Write down collected data in a new set of tables and plot the frequency characteristic on the same graph as above.

3. Differential Amplifier

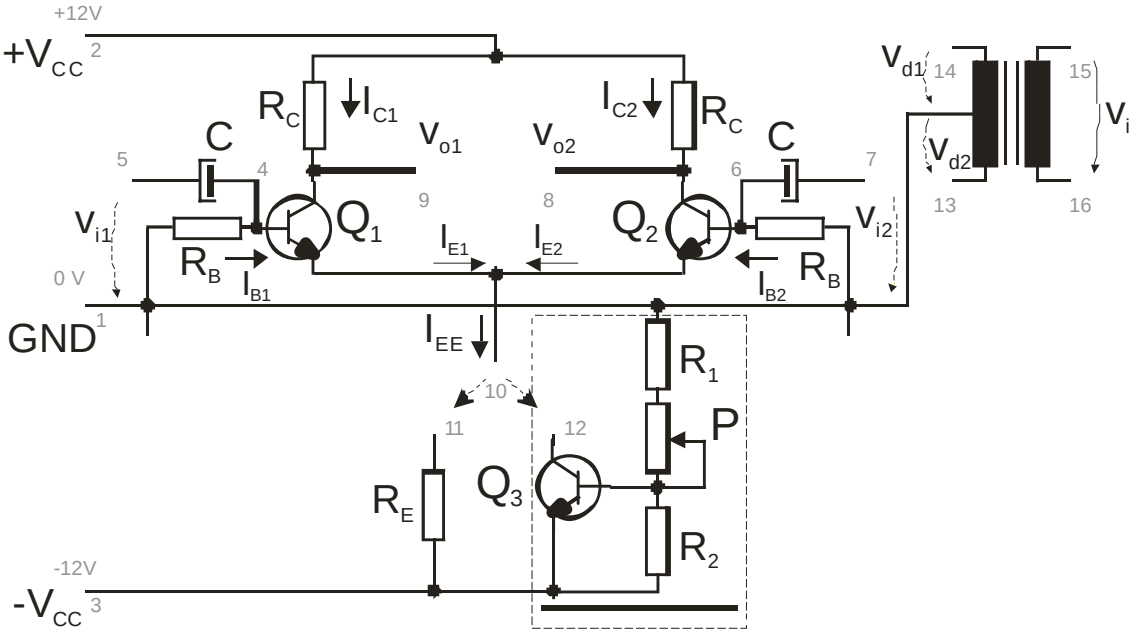
Introduction

The differential amplifier that amplifies mostly the difference between two input voltages having a common reference (usually the ground). The amplification of the mean of the two input voltages has to be very small. Using bipolar junction transistor technology, it is obtained by connecting two transistors having similar static characteristics, in a configuration like the one below:



Experimental Setup

The circuit board includes a differential amplifier that can be configured to use either a resistor in the emitters of the BJTs or a constant current source. A differential transformer having two identical secondary coils connected in series is also provided on the top right of the board, in order to provide two differential voltages when the primary is driven by a single-ended signal generator.



Measurements

Power the circuit board by connect a differential power supply between +Vcc, GND and –Vcc points. Set the differential voltage of the power supply to ±12 V.

Static operating point

Connect a DC milliammeter in series with the two emitters and the resistor R_E (points 10-11). Measure and write down the DC voltages in the bases, emmiters and collectors of the two transistors relative to ground. Check whether the DC voltages in the collectors of the two transistors are close to each other (<1 V), indicating that the two transistors have similar characteristics.

Differential amplification A_d

We aim at measuring the differential amplification by applying to the two amplifier inputs voltages whose instantaneous difference is different from zero, while the mean of the voltages is null. This corresponds to differential voltage $v_{id} = v_{i1} – v_{i2} \neq 0$ and common mode voltage $v_{ic}=0$. These equations can be fulfilled by two AC voltages that have identical RMS values but opposite phases. The RMS of the differential voltage is going to be $| v_{id} | = | v_{i1} | + | v_{i2} | = 2 | v_{i1} | = 2 | v_{i2} |$.

To obtain such a pair of differential voltages from a single-ended signal source, we use the differential transformer on the circuit board. Connect a single-ended signal generator output to the primary of the differential transformer (points 15-16). Connect the secondary coils (points 13 and 14) to the two amplifer inputs (points 5 and 7).

Measure either v_{i1} or v_{i2} (RMS) using a AC voltmeter and calculate $v_{id} = 2 v_{i1} = 2 v_{i2}$. Measure v_{o1} , v_{o2} (RMS) and calculate $v_{od} = v_{o1} + v_{o2}$

Take a set of v_{od} measurements for 5 different v_{id} values in the range 10–100 mV and fill in a table with the readings.

Calculate the differential amplification as the ratio between v_{od} and v_{id} , $A_d = v_{od} / v_{id}$.

Disconnect the R_{EE} resistor and connect the constant current source in the emitters of the two transistors. Repeat all the measurements above, fill in a new table with the results, and check whether you notice a significant difference between results.

Common-mode amplification A_c

For this step, we would like to measure the common mode amplification by applying to the two amplifier inputs voltages whose instantaneous difference is null, while the mean of the voltages is different from zero. This corresponds to applying a differential voltage $v_{id} = v_{i1} – v_{i2} = 0$ and a common mode voltage $v_{ic}=(v_{i1} + v_{i2})/2 \neq 0$. These equations can be fulfilled by two AC signals that have identical RMS values and same phase, in other words identical AC signals. The RMS of the common mode voltage is going to be $| v_{ic} | = | v_{i1} | = | v_{i2} |$.

Connect the two inputs together and to the output of the signal generator. The differential transformer is no longer used.

Using a AC voltmeter, measure $v_{ic} = v_{i1} = v_{i2}$. Measure v_{o1} , v_{o2} (RMS) and calculate $v_{oc} = (v_{o1} + v_{o2}) / 2$. Take 5 different v_{ic} values in the range 200–1000 mV and fill in a table with the v_{oc} readings.

Calculate the common mode amplification as $A_c = v_{oc} / v_{ic}$.

Disconnect the R_{EE} resistor and connect the constant current source in the emitters of the two transistors. Repeat all the measurements above, fill in a new table with the results, and check whether you notice a significant difference between results.

Common-mode rejection ratio CMRR

An ideal differential amplifier would have an infinite differential amplification and a null common-mode amplification. The ratio between A_d and A_c would be infinite. For a real amplifier, both values of the amplification would be different from the ideal values. To characterize using a single number how close is an actual amplifier to an ideal one, we define the common-mode rejection ratio (CMRR) as:

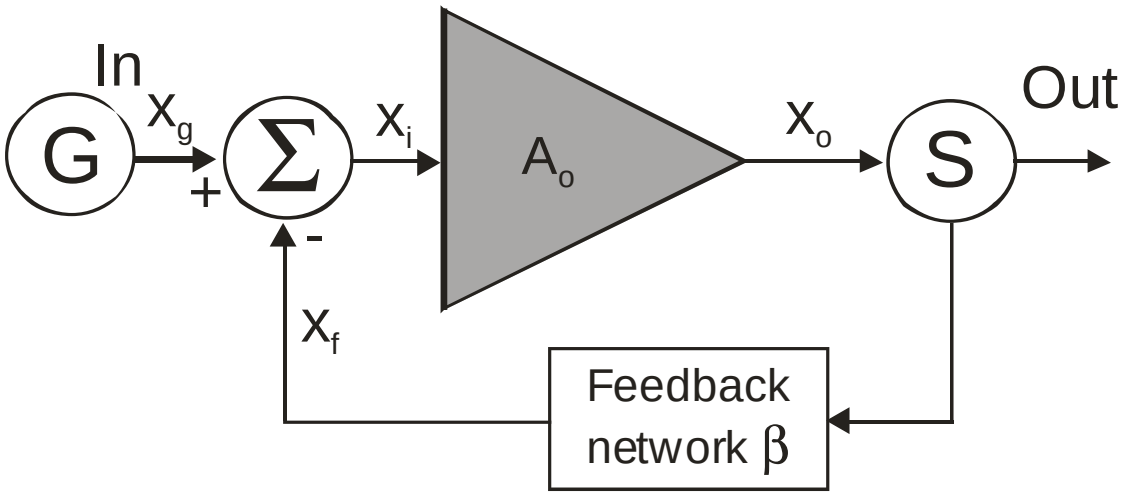
$$CMRR = A_d / A_c$$

For our amplifier circuit implemented with BJTs, take the largest A_d and the smallest A_c, measured in the circuit configuration with resistor R_{EE} connected in the emitters and calculate CMRR. Perform the same calculations for the configuration that uses the constant current source. Compare the two CMRR values and identify which configuration results in amplifier operation closer to the ideal one.

4. Feedback Amplifiers

Introduction

A feedback amplifier contains a loop through which a fraction of the output signal is fed back to the amplifier's input. The ideal circuit configuration of a *negative feedback* amplifier, where a fraction of the output signal is *subtracted* from the input signal is shown below:



The circuit is based on four elements:

- An amplifier having the open loop amplification $\mathbf{A_o}$.
- A sampling circuit **S** that reads the output
- A feedback network that processes the sampled output signal by dividing it, performing phase shifting, selective attenuation or some other operation. The transfer function of the feedback network is **β**.
- A summing circuit **Σ** that may add or subtract the feedback signal $\mathbf{x_f}$ to/from the input signal $\mathbf{x_g}$ from the generator **G**.

The amplification with negative feedback can be calculated as:

$$A_o = \frac{x_o}{x_i} \qquad x_f = \beta x_o \qquad x_i = x_g - x_f$$

$$A_f = \frac{x_o}{x_g} = \frac{x_o}{x_i + x_f} = \frac{x_o}{x_i + \beta A_0 x_i}$$

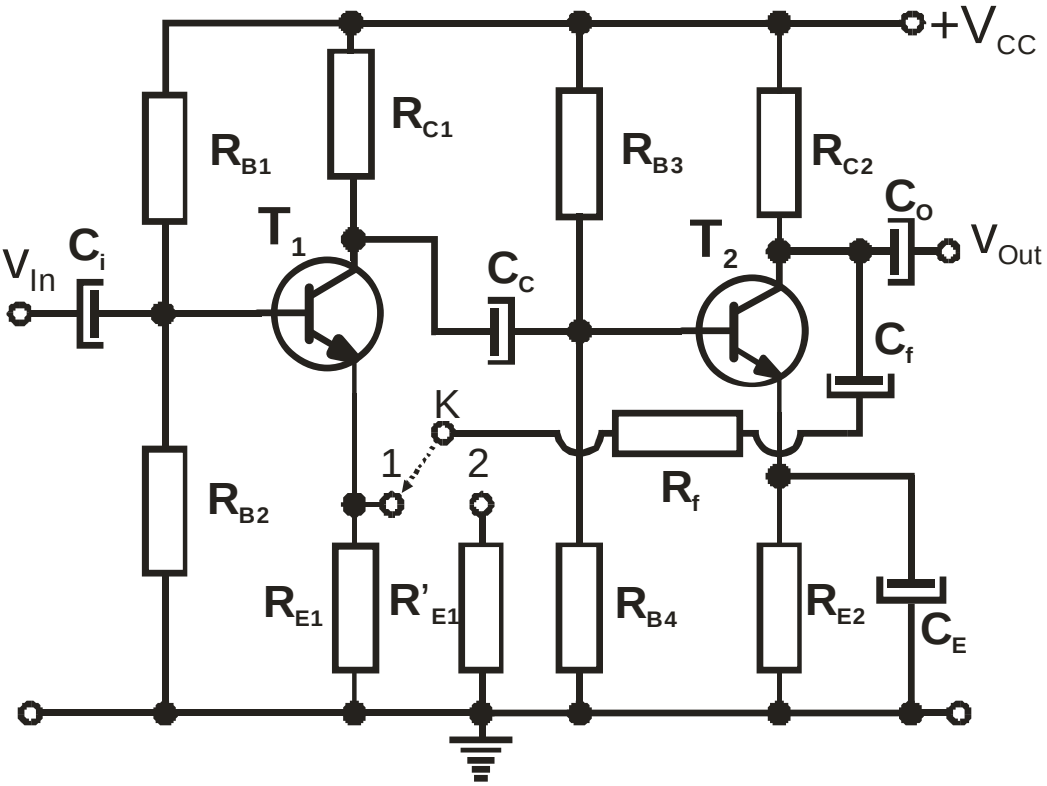
$$A_f = \frac{A_o}{1 + \beta A_0}$$

Negative feedback has several effects on the amplifier's operation:

- results in an amplification that is lower, but less susceptible to the amplifier's component dispersion.
- increases the bandwidth
- reduces distortion
- modifies the input and output impedance

Experimental Setup

In the laboratory, we will study the effects of negative feedback on the voltage amplification factor and on the frequency characteristic of a two-stage common-emitter BJT amplifier.



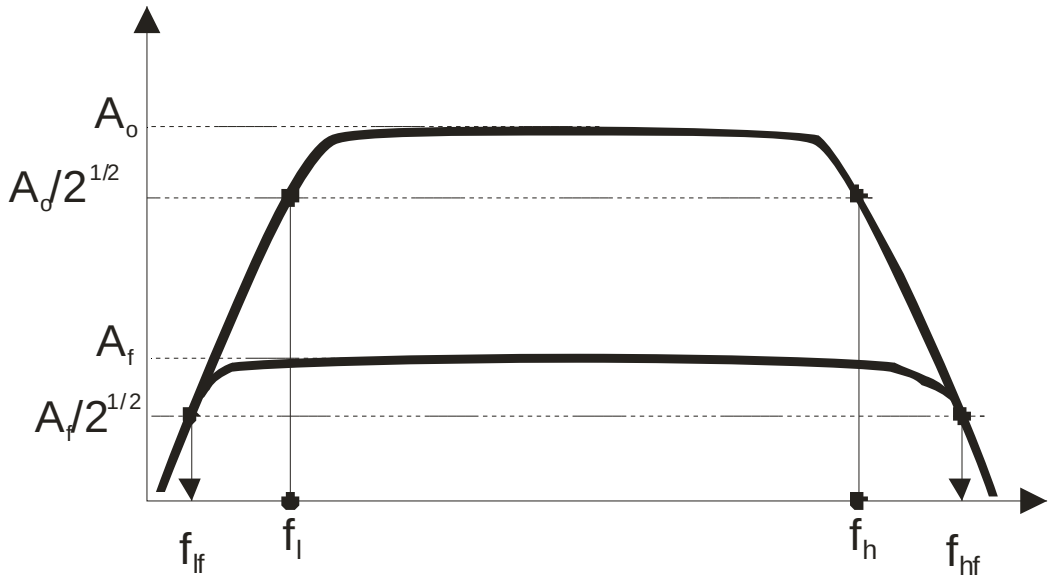
The feedback network is formed by the R_f and R_{E1} resistors, that form a resistive divider having a voltage ratio $\beta = \frac{R_f}{R_{E1}}$.

Effect of negative feedback on the amplification

> Power up the circuit board from a +12V power supply.
>
> Connect a signal generator at the input. Select a signal frequency of 1 kHz and an amplitude of 10 mV_{RMS}.
>
> Connect the K switch to pin 2, corresponding to open loop operation (no feedback).
>
> Measure with an AC millivoltmeter the signal amplitudes in the collectors of each transistor and calculate the voltage amplification A_{01} and A_{02} of each stage, as well as the total amplification A_0.
>
> Close the feedback loop by connecting the K switch to pin 1. Increase the amplitude of the signal to 100 mV_{RMS} and measure again the amplifications A_1 and A_2 of each stage, as well as the closed-loop amplification A_f. Which amplifications have been affected by the negative feedback?

Effect of negative feedback on the frequency characteristic

The frequency band of a negative feedback amplifier increases, compared to the open-loop bandwidth, as illustrated in the figure below:



The low and high cutoff frequencies with feedback change according to the equations:

$$f_{lf} = f_l(1+\beta A_o) \qquad f_{hf} = f_h/(1+\beta A_o)$$

Switch the circuit to open-loop operation mode (K connected to pin 2).

Select a 10 mV_{RMS} amplitude of the input signal. Determine the open-loop frequency characteristic of the circuit by measuring the output signal amplitude (using the AC millivoltmeter) while varying the frequency of the input signal in the 5 Hz … 5 MHz range, using a logarithmic frequency scale (f=5 Hz, 10 Hz, 20 Hz, 50 Hz, …., 1 MHz, 2MHz, 5MHz).

Calculate the low (f_l) and high (f_h) cutoff frequencies, at which the amplification drops to $A_0/\sqrt{2}$. The difference between the two frequencies is the open-loop bandwidth $B_0=f_h - f_l$.

Close the feedback loop by connecting K to pin 1.

Select a 100 mVRMS amplitude of the signal and measure the closed-loop frequency characteristic using the same procedure as used for the open-loop characteristic.

Calculate the low (f_{lf}) and high (f_{hf}) cutoff frequencies, at which the amplification drops to $A_f/\sqrt{2}$. Calculate the closed-loop bandwidth $B_0=f_{hf} - f_{lf}$.

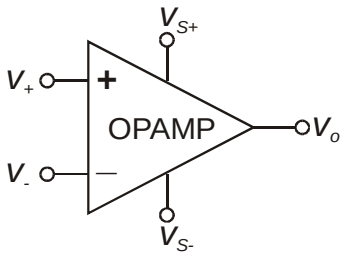
Plot both frequency characteristics on the same figure, using a double-logarithmic scale.

Check that the amplification x bandwidth product is approximately constant, for both open- and closed-loop operation.

5. Operational Amplifiers

Introduction

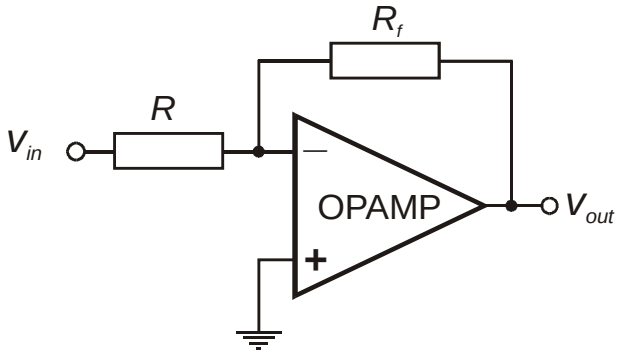
The operational amplifier is a DC-coupled differential voltage amplifier made on a single semiconductor chip, that has a high gain, high input impedance, and a low-impedance single-ended output, in most cases.



We will study the operation of various circuits built around the operational amplifiers.

Inverting amplifier

The inverting amplifier has a resistor connected in series with the inverting input and a feedback resistor between the output and inverting input. The non-inverting input is connected to ground.



The voltage amplification is:

$$A_V = -\frac{R_f}{R}$$

while the input impedance is:

$$Z_{IN} = R$$

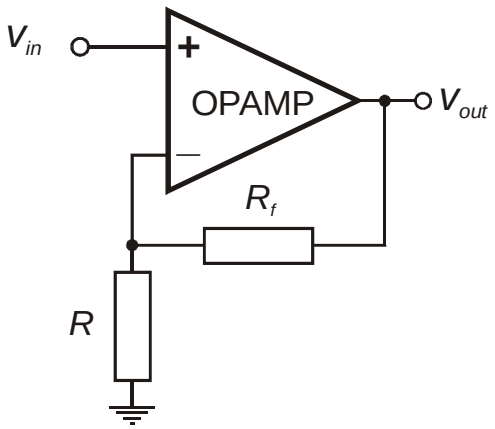
Power the circuit board from a ±6 V differential power supply.

To determine the DC input-output ***transfer characteristic*** of the circuit, the output voltage values for different input values have to be plotted. An on-board resistive divider allows the application of a variable voltage at the input. Please select about 10 input voltage values in the -2V – +2V range and write down the output voltage values. Measure both voltages using a DC voltmeter. Please make sure that the polarity of the signals is read, in addition to the absolute value. Plot $v_{out}=f(v_{in})$. Note the linear and the saturation region. By selecting a pair of points in the linear region, calculate the voltage amplification A_v and compare it to the theoretical value calculated based on the nominal values of the resistors.

To plot the ***frequency characteristic***, we have to apply at the input an AC voltage from a signal generator, having a peak amplitude in the linear region of the transfer characteristic and select different signal frequencies. Connect a signal generator at the amplifier's input, select a sine waveform having a RMS value of 500 mV (typical) and modify the frequency in the 1 Hz – 10 MHz. Use a logarithmic scale for the frequency, i.e. use values that follow the 1-2-5 template (1Hz, 2Hz, 5Hz, 10Hz, 20Hz, … , 1MHz, 2MHz, 5MHz, 10MHz). Using an AC voltmeter, read the output voltage value and calculate $A_v=v_{out}/v_{in}$ at each frequency. Plot A_v as a function of the frequency f in a double-logarithmic scale. As an option, calculate the voltage gain G in decibels as $G=20\log(A_v)$. Calculate the cutoff frequency at which the amplification drops to $A_0 / \sqrt{2}$ or the gain drops by 3dB of the maximal value.

Non-inverting amplifier

The non-inverting amplifier configuration includes a resistive divider connected between the output, the inverting input and ground. The circuit's input is the non-inverting operational amplifier input.



The voltage amplification of the non-inverting amplifier is:

$$A_V = \left(1 + \frac{R_2}{R_1}\right)$$

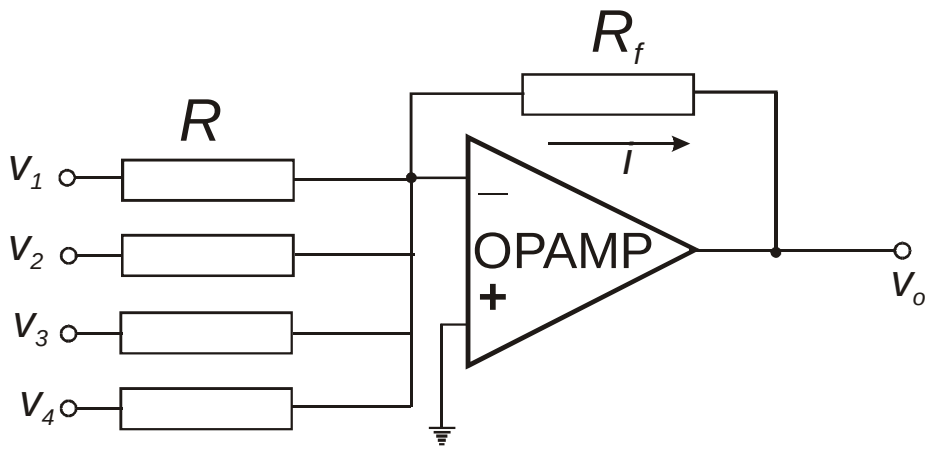
and an input impedance:

$$Z_{IN} = Z_{IN}^{OPAMP}$$

> Plot the DC transfer characteristic and the frequency characteristic, following the same steps as for the inverting amplifier.

Summing amplifier

The “operational amplifier” name originates from the early use of such devices in analog computers, for performing various mathematical operations. One application refers to the summation of several voltages. The summing amplifier is built on the basic inverting amplifier configuration, by adding more resistors in series with the additional inputs and the operational amplifier’s inverting input. The non-inverting input is connected to ground.



The output voltage is a sum of the input voltages:

$$v_o = -\frac{R_f}{R}\left(v_1 + v_2 + v_3 + v_4 + ...\right)$$

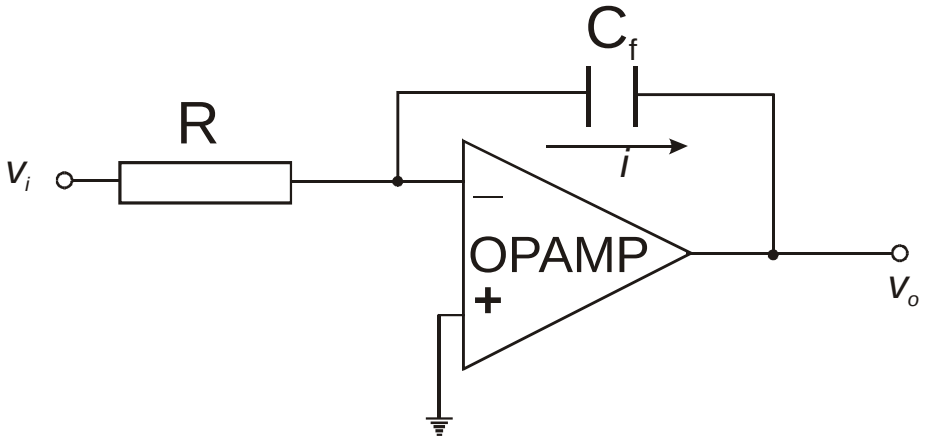
A version of the summation circuit includes different values of the resistors in series with the inputs, such that the formula above implements a weighted sum of the input voltages:

$$v_o = -R_f\left(\frac{v_1}{R_1}+\frac{v_2}{R_2}+\frac{v_3}{R_3}+\frac{v_4}{R_4}+....\right)$$

> The circuit board in the lab implements a two-input version of the summation amplifier and two resistive dividers that allow the application of different DC voltages at the inputs. Power the circuit and apply different combinations of the input voltages (about 5 different values in the +/- 0.5V DC range), verifying the value of the output voltage with the theoretical value based on the values of the resistors and input voltages, using the formula above.

The integrator

The integrator performs an even more complex mathematical operation using a very simple circuit configuration that is based on the inverting amplifier, where the feedback resistor is replaced with a capacitor.



The output waveform is given by the equation:

$$v_o = -\frac{1}{C_f R}\int v_i(t)dt$$

> As the equation describing circuit's operation implies, the circuit's analysis is meaningful only in AC. We will therefore plot in first place the frequency

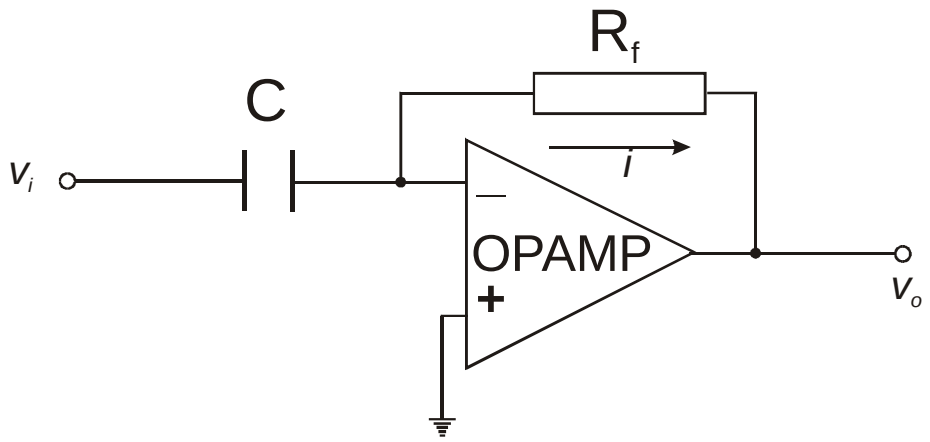
characteristic of the circuit $A_v = A_v(f)$. Connect a signal generator at the amplifier's input, select a sine waveform having a RMS value of 500 mV (typical) and modify the frequency in the 1 Hz – 10 MHz. Use a logarithmic scale for the frequency, i.e. use values that follow the 1-2-5 template (1Hz, 2Hz, 5Hz, 10Hz, 20Hz, … , 1MHz, 2MHz, 5MHz, 10MHz). Using an AC voltmeter, read the output voltage value and calculate $A_v=v_{out}/v_{in}$ at each frequency. Plot A_v as a function of the frequency f in a double-logarithmic scale. As an option, calculate the voltage gain G in decibels as $G=20\log(A_v)$.

Calculate the cutoff frequency at which the amplification drops to $A_0 / \sqrt{2}$ or the gain drops by 3dB of the maximal value.

To verify that the circuit performs an integration of the input waveform, we have to select a different waveform, as by integrating a sine function, we obtain a cosine function, which has identical appearance, but different phase. We therefore configure the signal generator to output a square function. The integral of a square function should be a triangle waveform. Connect a dual-channel oscilloscope at the input and output, to visualize the signal waveforms. By looking at the frequency characteristic of the circuit determined at the previous step, for a sine input waveform, select two frequencies, one on the flat region of the characteristic, the other one on the negative slope of the characteristic. Check on which region of the frequency characteristic the circuit performs the intended signal processing. Consider generalizing the results in that that any circuit having a similar frequency characteristic acts as an integrator.

The differentiator

The differentiator performs another complex mathematical operation using a very simple circuit that is based on the same inverting amplifier configuration, where the input resistor is replaced with a capacitor.



The output voltage is:

$$v_o = -R_f C \frac{dv_i}{dt}$$

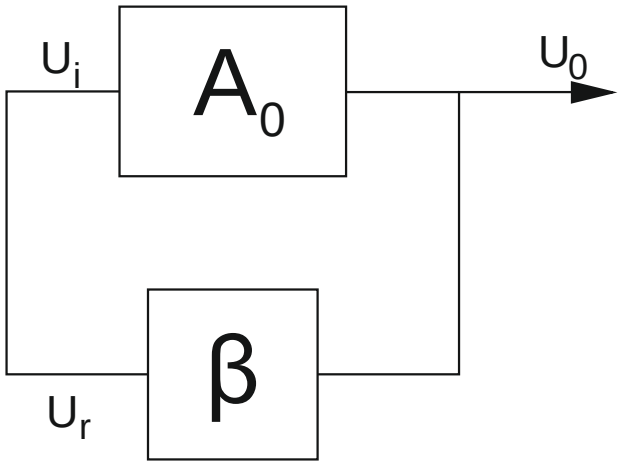
Plot the frequency characteristic of the differentiator circuit $A_v = A_v(f)$, using the same methodology as for the integrator. Please note the positive and negative slope regions of the characteristic, in addition to the flat region.

By selecting a triangle input signal, verify the intended operation of the circuit as differentiator. The signal obtained by differentiating a triangle waveform should be a square waveform. Check the operation at three frequencies, one on the positive slope region of the frequency characteristic, the other one on the flat region, and the third one on the negative slope region. Consider generalizing the results in that that any circuit having a frequency characteristic presenting a region with positive slope acts as a differentiator for signals in that frequency range.

6. Oscillators

Introduction

The most common form of an electronic oscillator consists in an amplifier connected in a positive feedback loop, as illustrated in the figure below. The amplification factor within the open loop is A_0, and the transfer function of the feedback network is β.



For the feedback amplifier to operate as an oscillator, an output voltage v_0 must be present without the application of an external signal at the input. For an input voltage v_f, the output voltage is:

$$v_0 = A_0 v_r$$

But

$$v_r = \beta v_0$$

Then

$$u_0 = A_0 \beta u_0$$

$$A_0 \beta = 1$$

This is the condition for the feedback amplifier to function as an oscillator. The condition is called the *Barkhausen stability criterion*, named after the German physicist Heinrich Georg Barkhausen (1881–1956) that introduced it in 1921.

Since A_0 and β are generally complex numbers, this condition must be fulfilled both in modulus and in phase. Thus the $A_0\beta = 1$ condition implies:

$$|A_0||\beta| = 1$$

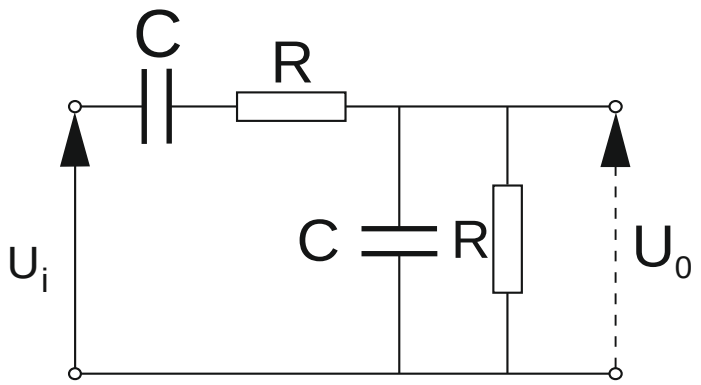
And

$$\arg(A_0\beta) = \arg(A_0) + \arg(\beta) = 2k\pi, k\epsilon\mathbb{Z}$$

The amplifier has in general constant phase characteristics, $\arg(A) = 0$ (non-inverting amplifier) or $\arg(A) = \pi$ (inverting amplifier) at the frequencies at which we want to obtain oscillations. The feedback configurations can vary largely. They all have to fulfill the phase condition exactly at the frequency where the oscillations will occur, the amplitude condition $|A_0||\beta| = 1$ being obtained through the variation of the amplification A_0. There can be 2 types of feedback networks: LC-based or RC-based.

RC Oscillators

Out of the several types of RC circuit configuration, including RC phase-shifting circuit, the double-T circuit, the Wien circuit etc., we will study in detail the Wien configuration, shown below:



The transfer function of the Wien circuit is:

$$\beta_{(w)} = \frac{\frac{R}{j\omega C}}{R + \frac{1}{j\omega C} + \frac{\frac{R}{j\omega C}}{R + \frac{1}{j\omega C}}} = \frac{1}{3 + j(\omega RC - \frac{1}{\omega RC})} = \frac{3 - j(\omega RC - \frac{1}{\omega RC})}{9 + \left(\omega RC - \frac{1}{\omega RC}\right)^2}$$

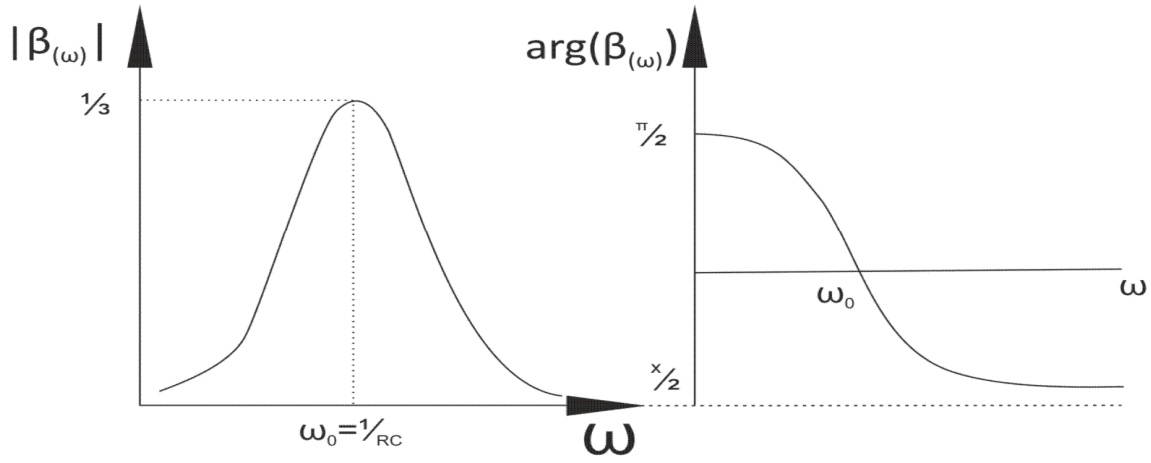
The transfer function argument is

$$\arg(\beta_{(\omega)}) = \frac{1}{3} arctg(\frac{1}{\omega RC} - \omega RC)$$

And the modulus:

$$|\beta_{(\omega)}| = \frac{1}{\sqrt{9 + (\omega RC - \frac{1}{\omega RC})^2}}$$

The argument and the modulus of the transfer function of the Wien system are plotted in the figures below:



The phase shift is null for $Im(\beta) = 0$, or:

$$\omega RC = 1$$

The RC oscillator can therefore only operate at a frequency where the phase condition is met:

$$\omega_0 = \frac{1}{RC}$$

In addition to meeting the phase condition in the Barkhausen stability criterion, in order for the amplitude condition to be fulfilled as well, the amplification factor A_0 has to meet the criterion:

$$|A_0||\beta_{(\omega)}| = 1$$

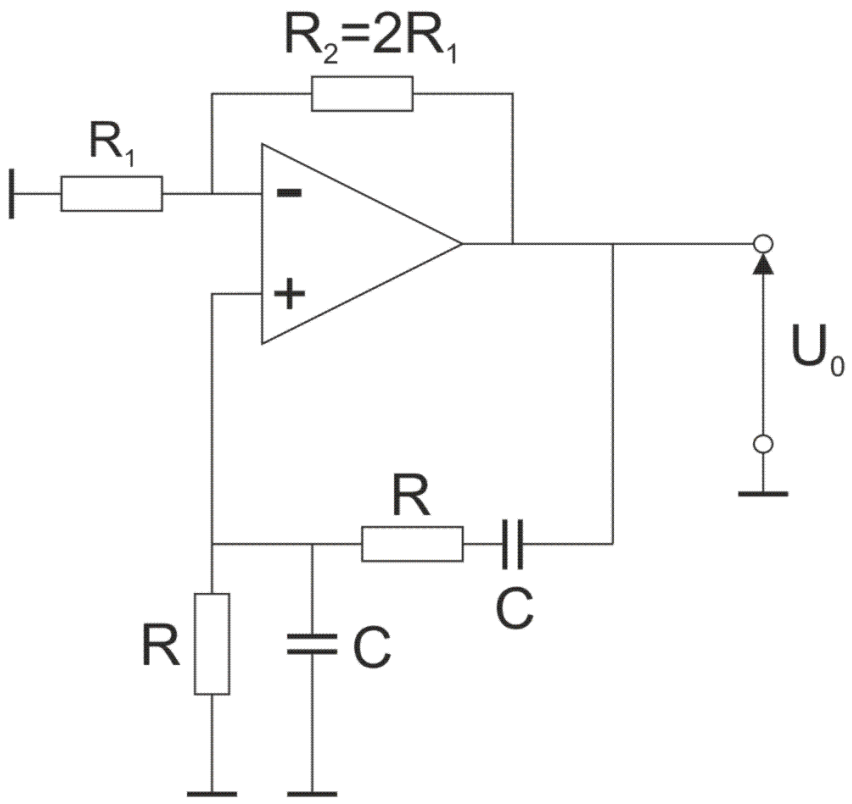
The modulus of the transfer function at this frequency is:

$$|\beta_{(\omega_0)}| = \frac{1}{3}$$

The amplitude condition will require for the amplification frequency A_0 to be equal to 3, such that:

$$|A_0|\left|\beta_{(\omega_0)}\right| = 3\frac{1}{3} = 1$$

We can build an oscillator with an operational amplifier in a non-inverting configuration and $A_u = 1 + \frac{R_2}{R_1} = 3$, using a circuit schematics as illustrated below:



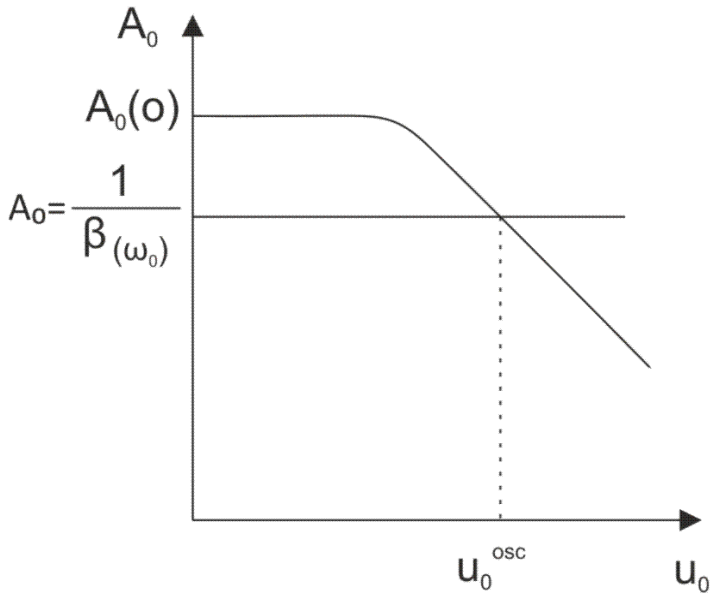
Barkhausen stability criterion does not provide any information about the output amplitude level. If we look at the oscillator as a positive feedback amplifier, when Barkhausen condition is met its feedback amplification becomes infinite and therefore the signal at the output may become infinite. However this cannot happen in practice due to the limited output voltage range, within the power rail voltage.

The oscillation amplitude has a finite value due to the non-linearity of the amplification, which decreases with higher output voltage:

$$A = A_{(u_0)}$$

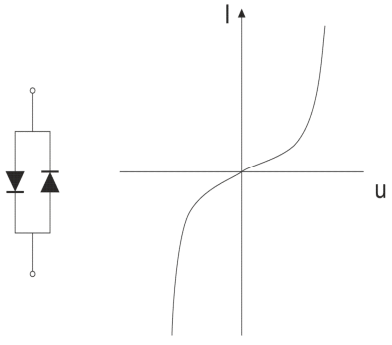
If the output voltage amplitude increases significantly, the amplifier output saturates, the amplification drops to the point the Barkhausen condition can no longer be met. As a matter of fact, the oscillation amplitude stabilizes at a specific

output voltage u_0^{osc} at which the modulus of the amplification drops to exactly $\frac{1}{|\beta|}$. Therefore, on powering up the circuit, the output voltage increases quickly to u_0^{osc}, at which the amplification drops and the Barkhausen condition is met (as illustrated in the figure below).



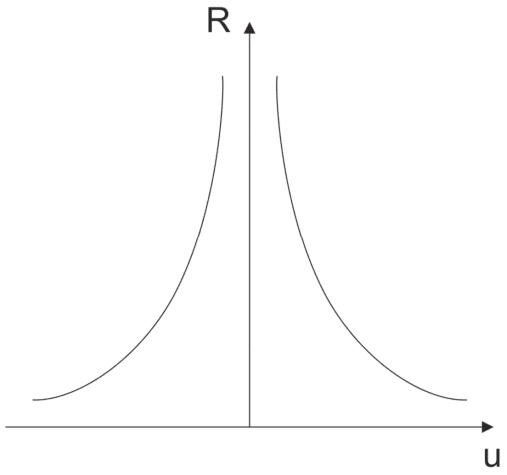
In many instances, it is preferred to intentionally introduce non-linear elements in the circuit to limit the amplification and the output signal before the amplifier naturally limits the signal. The advantage of these circuits, called amplitude limiters, is that they can be designed in such a way to limit the output signal in a controlled way, with a reduced signal distortion.

One the most simple limiter circuits uses the non-linear I-V characteristic of the semiconductor diodes. To obtain a limitation on both polarities, two diodes must be installed in an anti-parallel configuration, with the resulting current-voltage characteristics:

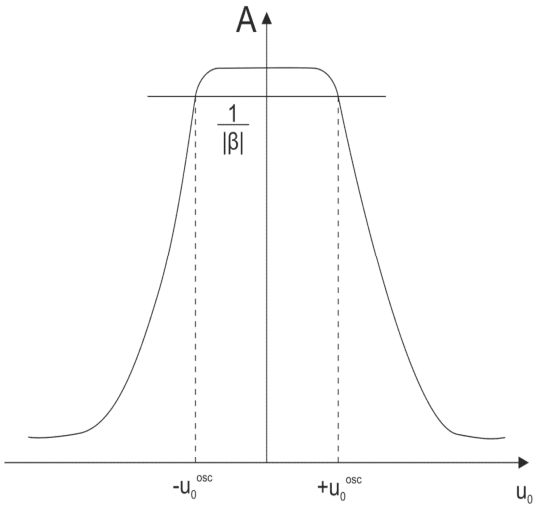


By including this circuit in the negative feedback loop of an operational amplifier, the amplification will be proportional with the dynamic resistance of the diodes. The

dynamic resistance of the diodes will be the tangent of the slope of the current-tension characteristic and will be depending on the voltage applied to the circuit:

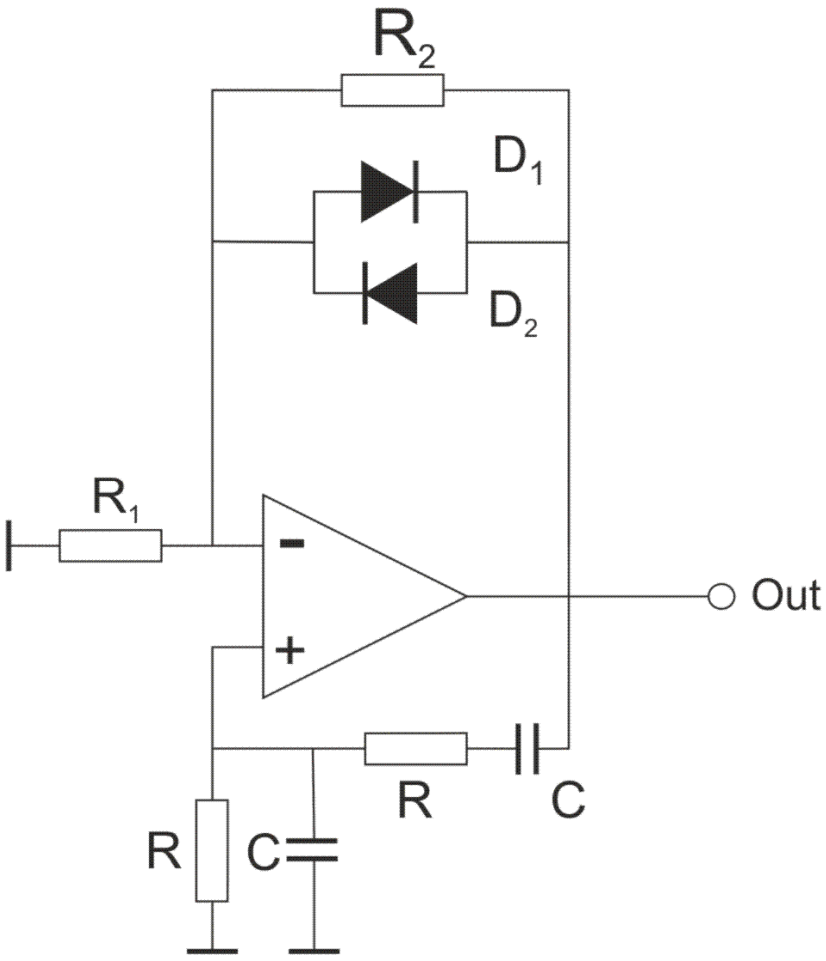


Installing in parallel with the diodes a resistance R, the amplification voltage dependence at the output will become:



It can be seen that Barkhausen condition is met only at a specific output voltage.

A complete oscillator with the Wien network and a limiter circuit will have following schematics:



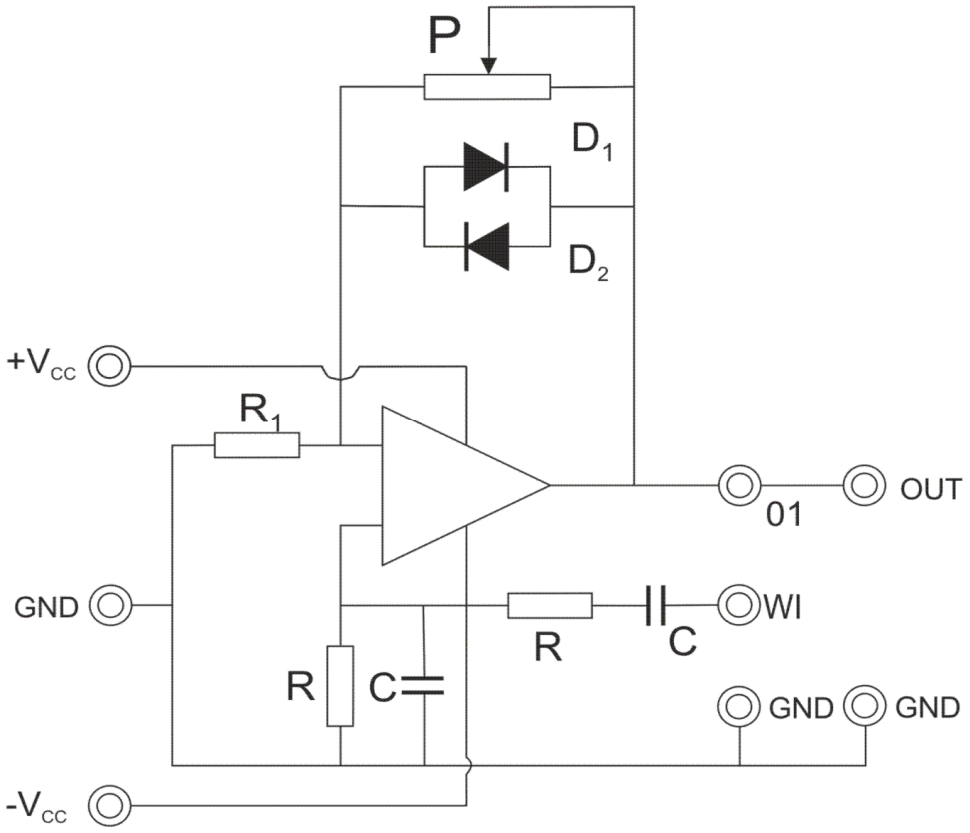
Other voltage-limiting circuits may use varistors, baretors, thermistors, field effect transistors, etc.

Experiment

The experimental setup consists in a circuit board that can be used for studying the frequency transfer function of the Wien network and also for studying the operation of an oscillator built around this network.

By applying signal from one signal generator to the WI input of the Wien system (point O1 and WI have to be disconnected), the circuit operates like a non-inverting amplifier which amplifies the signal from the output of the Wien network. If potentiometer P is in the leftmost position, where its resistance is null, the limiter circuit is short-circuited and the amplifier becomes a voltage follower, the output voltage being the same as the output voltage of the Wien network, allowing for the measurement of the feedback network transfer function.

By connecting the input of the Wien network to the output of the amplifier, we close the positive feedback loop. Initially, with the potentiometer P in the leftmost position (A_v=1), the amplitude condition in the Barkhausen stability criterion is not met. By slowly rotating the potentiometer P in the clockwise direction, the amplification reaches at some point A_v=3, when the Barkhausen's condition is met, oscillations appear with rapidly increasing amplitude, to the point where the amplitude-limiting circuit starts operating.



1. Power the circuit using a differential power supply, applying a differential voltage of +/-6 V to the +/-V_{cc} pins.
2. Connect to the WI input of the circuit to the output of a sinusoidal signal generator. Connect an AC milivoltmeter at the output.
3. Turn the potentiometer P in the counter-clockwise direction, as indicated in the figure, until it reaches the leftmost position. The amplifier will become a voltage follower and will replicate the voltage present at the ouput of the Wien network.
4. Measure the frequency transfer function $\beta = \beta(\nu)$ of the Wien network and then graphically represent it in a logarithmic scale:

$$\left|\beta_{(v)}\right| = \frac{u_0}{u_i} = f(\log(\mathrm{v}))$$

In the v = 20 ... 2000 Hz frequency range. The position of the maximum, v_0, must be found.

5. Adjust the generator to the frequency v_0 previously calculated, at which the Wien network transfer function takes the maximal value. Turn the potentiometer P in the clockwise direction, to its rightmost position.
6. To put into evidence the operation of the voltage-limiting circuit, plot the voltage transfer characteristic of the amplifier, $v_o = f_{(v_i)}$. Apply a v_i input voltage in the range $v_i = 0{,}1 \ldots 1{,}5\ V$, in 0.1 V increments.
7. From the previously measured data calculate and plot the amplification $A = \frac{v_0}{v_i}$ versus the input voltage v_i .
8. Disconnect the signal generator. Rotate the potentiometer P back to the its leftmost position, and connect the 01 and WI points together.
9. Slowly rotate the potentiometer in the clockwise direction and observe the onset of the oscillations, using an oscilloscope connected to the output. Using the oscilloscope, measure the period T_{osc} of the output sine wave, then calculate the frequency $v_{osc} = \frac{1}{T_{osc}}$, and compare it with the frequency v_0 determined at point 4 above, corresponding to the maximal value of the Wien transfer function.

LC Oscillator with Common Base Transistor

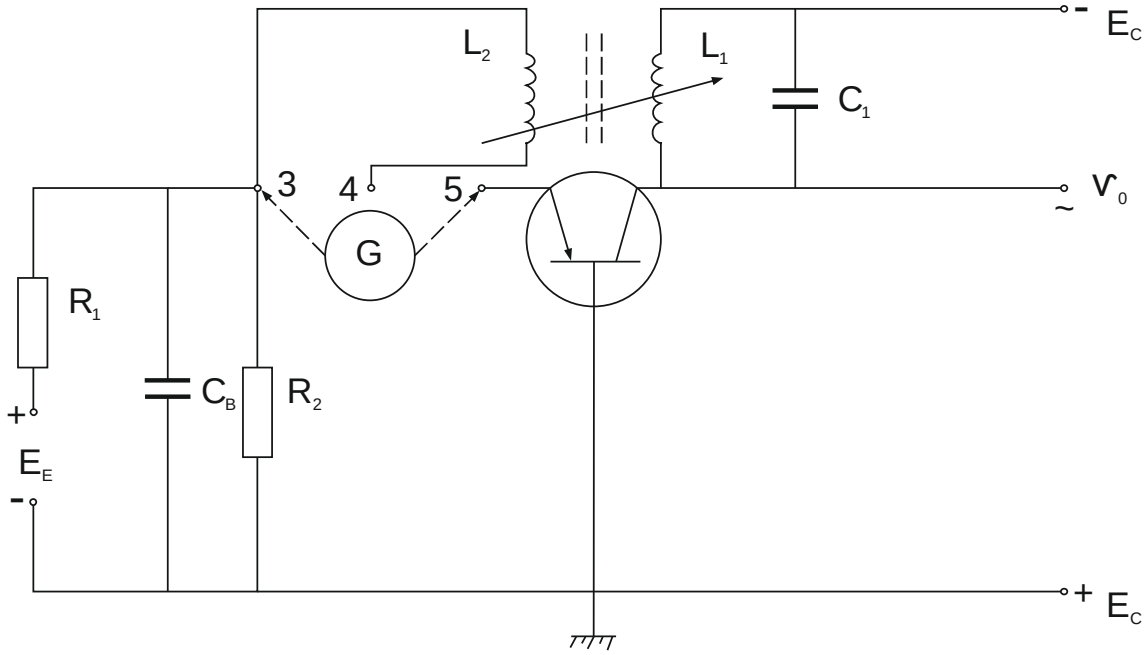
Experimental setup

A selective amplifier based on an LC circuit board in the laboratory can be transformed into an oscillator through an inductive-coupled feedback circuit.

The L_1C_1 circuit represents the load of the common base BJT amplifier, having a resonance frequency around 35 KHz. Emitter-base DC bias voltage is applied through a resistive divider formed by R_1 and R_2 and connected to ground in AC through the capacitor C_E. When operating as frequency-selective amplifier, the signal generator must be coupled between points 3 and 5. To operate as oscillator, a shunt must be placed between points 4 and 5.

Experiment

The circuit must be powered using voltages $E_c = 12\ V$ and $E_E = 9\ V$, with a polarity as shown below.



a) When operating as a selective amplifier, a frequency generator must be connected between points 3 and 5, having a voltage amplitude set to 20 mV. The frequency characteristic $\vartheta_0 = f(\upsilon)$ has to be plotted, by varying the frequency in the 20kHz through 50 kHz range.
b) When operating as an oscillator, the generator is disconnected and point 4 is connected to point 5.

By varying the inductive coupling factor between L_2 and L_1 , we can evidence several aspects of the operation of the circuit as an oscillator. Please note the following:

- The circuit oscillates only if the phase condition is met
- There exists an optimal coupling factor, for which we obtain an output sine signal having minimal distortions.
- The operating frequency is approximately equal to the LC circuit resonance frequency
- If the coupling factor increases, the output voltage will be distorted.

For the visualization of the signal form and the measurement of the output frequency, an oscilloscope has to be connected at the output.

7. Multivibrators

Introduction

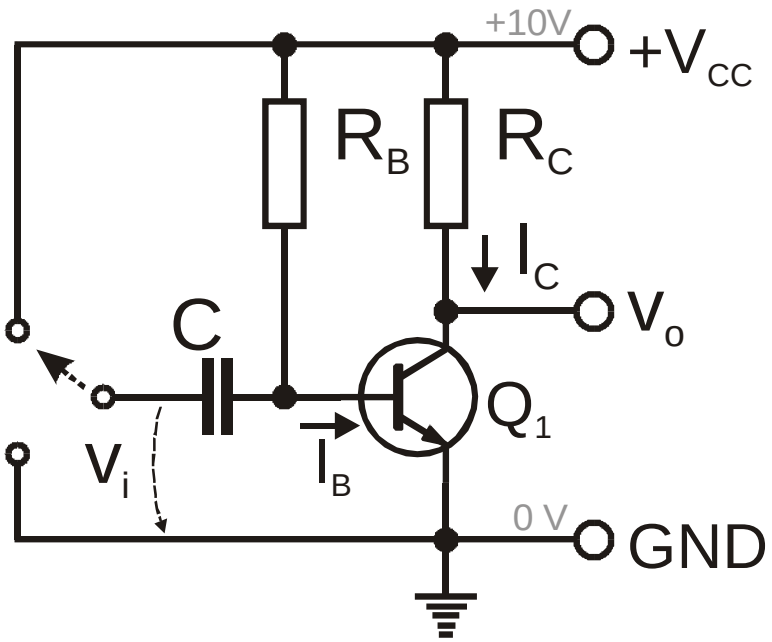
Multivibrators are switching circuits that can be categorized as:

- monostable, whose output has a single stable state, and temporarily switches to the complementary state when driven by an external trigger signal;
- astable, that switch continuously between complementary states at a fixed frequency (free-running);
- bistable, that can indefinitely stay in either state, unless an external trigger pulse is applied, flipping the circuit in its complementary state

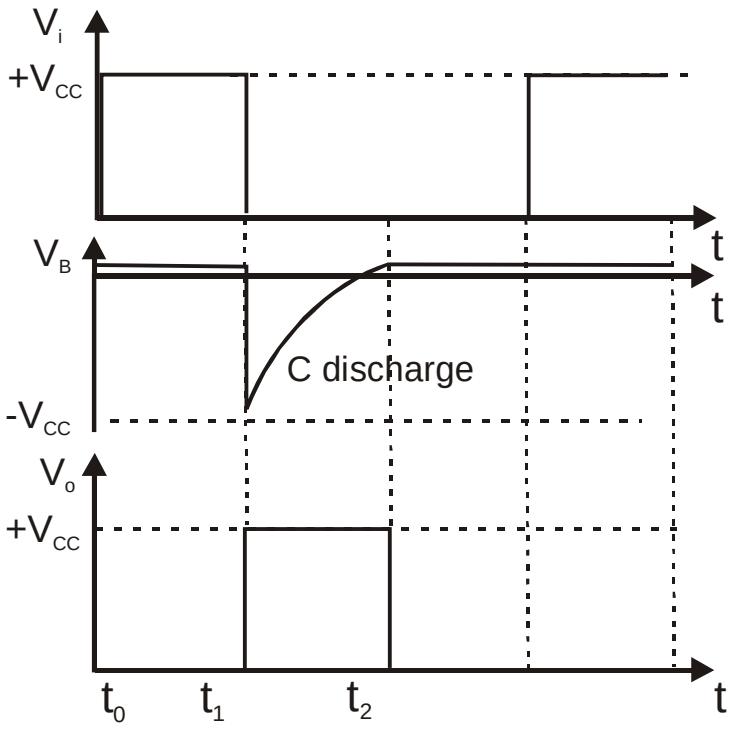
Being switching circuits, they generate square waves that contain a lot of harmonics, and that's where the "multivibrator" name originates from.

Monostable multivibrator

The monostable circuit in its implementation using bipolar junction transistors (BJT) is shown below:



At rest, the base of the BJT is pulled up through RB, such that the Q_1 transistor is in saturation state, therefore the output voltage takes a low value ($V_{CE}^{sat} \approx 0.2V$ for a Si BJT). By connecting the input to $+V_{CC}$, the capacitor charges with V_{CC}-V_{BE}. When



connecting the input back to ground, the charged capacitor will apply a negative –(V_{CC}-V_{BE}) voltage on the base of the transistor, initially, switching off the Q_1 transistor. As a result, the output goes high, being pulled up by the R_c resistor. However, the capacitor C will not preserve its charge, and will start charging through the R_B resistor following an exponential law, until it reaches again the V_{BE} threshold for switching on the transistor. At this point the output goes low again and remains in this state until a new trigger signal is applied.

During the capacitor discharge phase [$t_1 \ldots t_2$], the base voltage is:

$$V_B = V_{CC} - (2V_{CC} - V_{BE}^{sat})e^{-\frac{t}{R_b C}}$$

The duration of the output pulse is the duration required for V_B to reach V_{BE}^{sat} at which the transistor is switched back on:

$$T = R_B C \ln\left(\frac{2V_{CC} - V_{BE}^{sat}}{V_{CC} - V_{BE}^{sat}}\right),$$

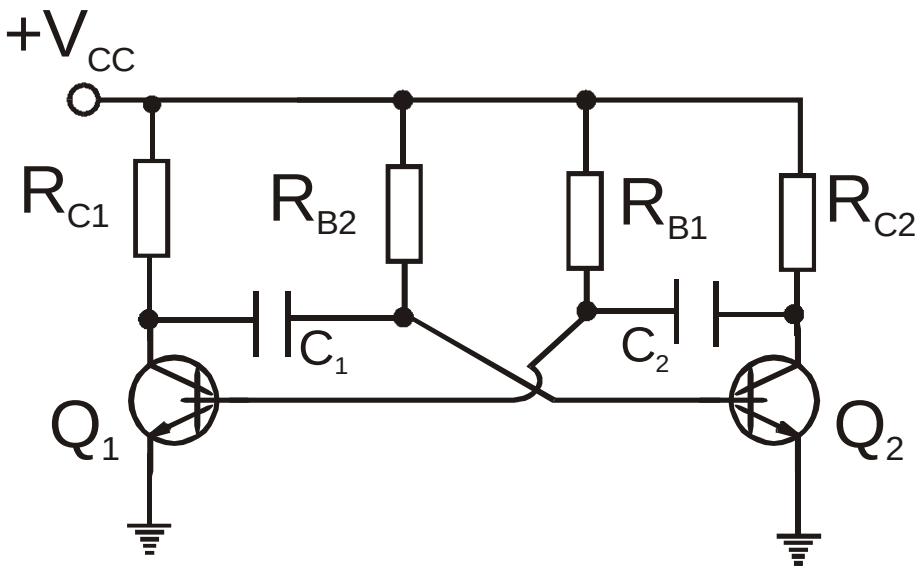
Which, for $V_{CC} >> V_{BE}$ can be approximated with:

$$T = t_2 - t_1 \approx R_B C \ln(2) \approx 0.69 \cdot R_B C$$

> To study circuit's operation, power the circuit board from a +10V power supply. Two capacitors in series with the base of the transistor of C_1 = 10 μF and C_2 = 47 μF are available. By manually connecting the input to +VCC, to charge the capacitor, followed by connecting the input to GND, a trigger pulse is applied. The LED in the collector of the transistor will go off for a few seconds. Confirm that the duration of the output pulse is at least 4 times longer for the larger capacitor (C_2) than for the smaller capacitor (C_1). Given the fact that the RB is 100k, calculate the correspondence between the measured durations and calculated time constants for each capacitor.

Astable multivibrator

The astable circuit is obtained by connecting two monostable circuits in series and closing the loop by connecting the output of the second monostable to the input of the first monostable circuit. Modifying the layout of the schematics by mirroring the second monostable multivibrator, we obtain the following representation of the astable circuit:



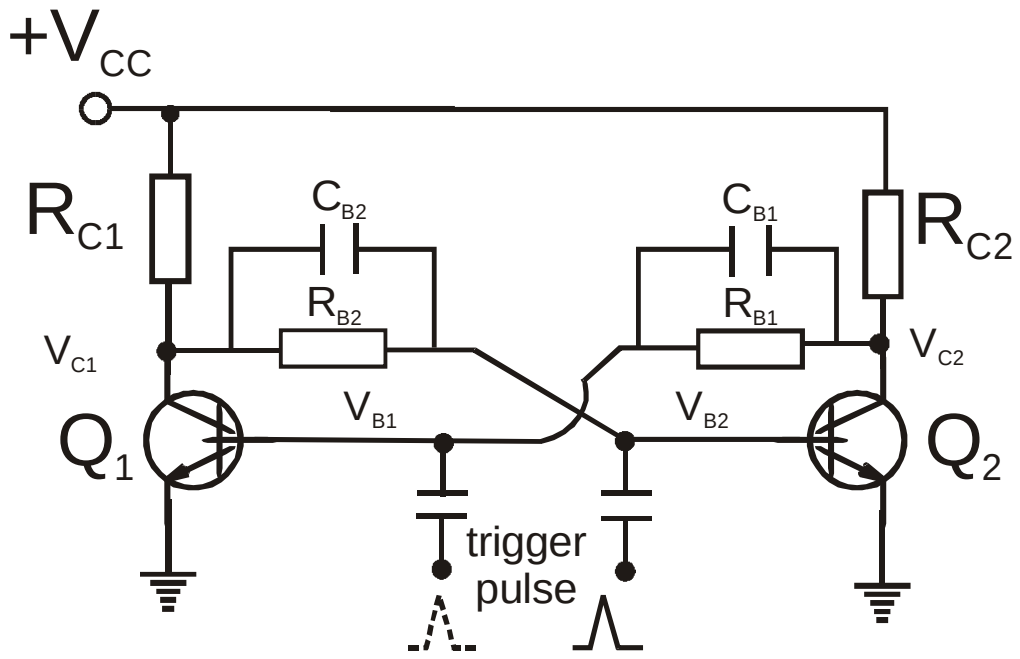
> Connect the second monostable on the circuit board in the lab in series with the first one. By applying a trigger pulse at the input of the first monostable, observe the operation of the series circuit. Close the loop by connecting the output of the second monostable to the input of the first one. Observe the

continuous flipping of the states as one monostable drives the other one, in the absence of any trigger signal.

To visualize the waveforms in various points of the circuit, use the high-frequency astable circuit built on the bottom-right side of the board. Visualize V_{B1}, V_{C1}, V_{B2}, V_{C2} on the oscilloscope screen, two at a time. Measure the time constants of each monostable stage that forms the astable multivibrator.

Bistable multivibrator

The bistable circuit is a modification of the astable circuit obtained by disconnecting the resistors pulling the bases of the transistors to VCC and connecting them to the collector of the opposite transistor (in parallel with the capacitors in series with the bases). The bistable circuit is shown below:



In this circuit configuration, any transistor that is in the on state will pull down the base of the other transistor. The other transistor will be in OFF state, such that the collector will be pulled up through the collector resistor. However, the high voltage on this transistor will keep the first transistor in the ON state, through the corresponding R_B resistor. As a result, the circuit will preserve its current state. To change state, a trigger pulse will have to be applied to the bases of the two transistors, through the decoupling capacitor in series with the trigger pulse. The two capacitors in series with the trigger input can be connected together. By performing a careful circuit

analysis when applying a raising trigger pulse, one can see that the transistor that is in the OFF state will be flipped to the on state, while the effect on the transistor that is already ON state will be null. Through the same feedback mechanism that preserves bistable's state, with the help of the charged stored on the capacitors, the circuit flips to the complementary state. The process goes on in a very similar way for the other transistor, on the next trigger pulse.

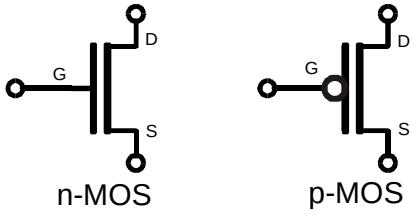
By triggering the bistable on the bottom right side of the circuit board in the lab using the low frequency astable circuit (formed by connecting in series the two monostable circuits on the top of the board), observe the operation of the circuit. Note that the cycle time of the LED's in the collectors of any of the transistors in the bistable circuit is twice the cycle time of the monostable circuit. In other words, the switching frequency of the bistable is half the frequency of the circuit driving it.

> Disconnect the low frequency astable circuit and drive the bistable circuit from the any of the outputs of the high-frequency astable circuit on the bottom-right of the circuit board. Connect a dual-channel oscilloscope at the trigger input and at one of the bistable circuit's output. Please note the operation of the circuit as a frequency divider with a factor of 2.
>
> Make hand sketches of the waveforms for all three multivibrator circuits you have studied.

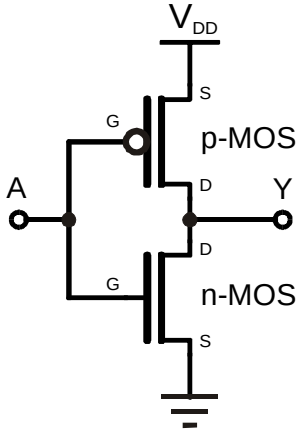
8. CMOS Logic Gates

Introduction

Logic gates implemented using complementary metal-oxide-semiconductr (CMOS) transistors represent the fundamental building blocks of most of the modern digital circuits. The word “complementary” refers to the fact that the CMOS uses pairs of p-type MOS transistors and their counterpart, n-type MOS transistors. The technology currently allows obtaining highest speeds and lowest dissipated power, being used in most modern microprocessors.



The simplest CMOS circuit is the inverter, which has the schematics shown below:



Two complementary transistors (n-MOS and p-MOS) are connected in series, having the gates (G) and drains (D) connected together. The source (S) of the n-MOS

transistor is connected to ground (labeled GND or V_{SS}), while the source of the p-MOS transistor is connected to a the power supply (V_{DD}) that needs to supply a voltage greater than the gate threshold voltages (V_T) of any of the transistors. The gates of the transistors represent the input (A), while the drain represent the output of the circuit (Y).
When the voltage on the A input is null, the voltage on the n-MOS transistor is below the threshold voltage, therefore the transistor is in "OFF" state. Its drain-source circuit behaves as an open switch. However, the voltage applied on the p-MOS transistor is $-V_{DD}$, whose magnitude is greater than the threshold voltage V_T, bringing the p-MOS transistor in the "ON" state. The drain-source circuit can be considered a closed switch. Therefore, the Y output will be pulled by the p-MOS transistor to a high level, close to V_{DD}.
If a high voltage level ($\sim V_{DD}$) is applied at the input A, using a similar line of reasoning, one can see that the n-MOS transistor will be in the ON state, while the p-MOS transistor will be in the OFF state. Correspondingly, the Y output will be pulled low by the n-MOS transistor, to a voltage close to 0 (GND).
If we attribute to all voltages having a low value (e.g. less than $V_{DD}/2$) a logical value of FALSE (or binary 0), and to all high voltages (close to V_{DD}) the logical value TRUE (or binary 1), we can build the **truth table** of the circuit, where the output values for all input logical levels (and all possible combinations of input levels, for a multiple-input circuit) are shown:

A	Y
0	1
1	0

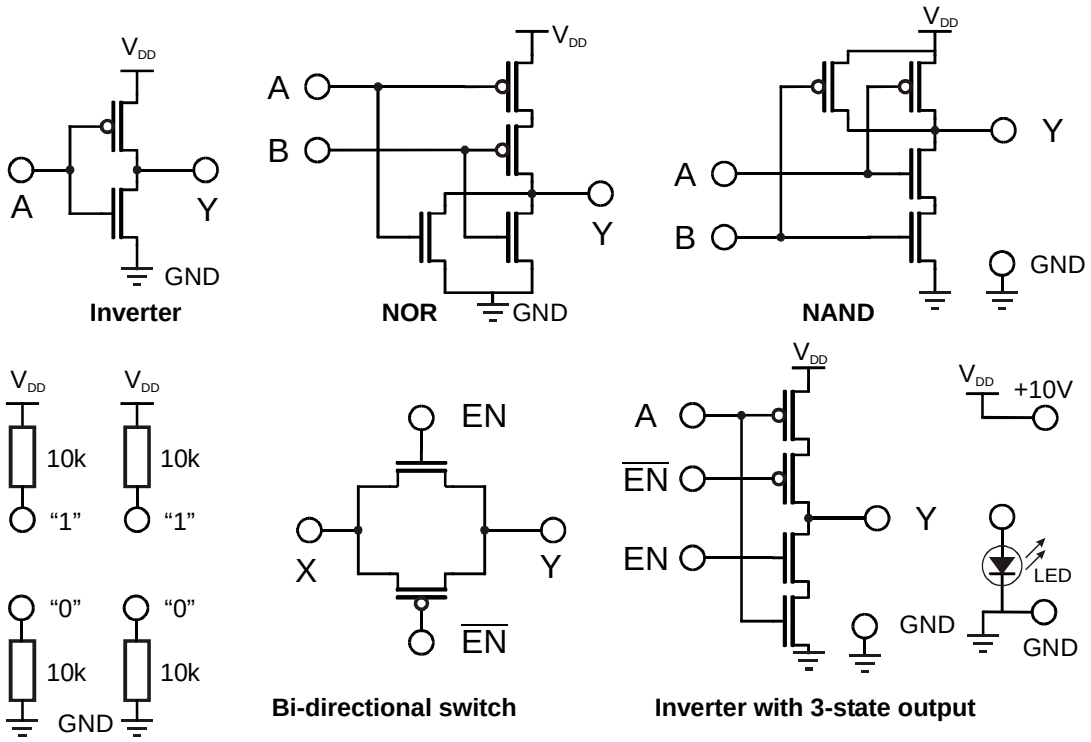
We can see that the logical state of the output is always opposite to the logical state of the input, leading to naming the circuit as "inverter". The logic function of this circuit is the **negation**, or **logical complement**:

$$Y = \overline{A}$$

One has to note that the inverter circuit has a remarkably simple structure, containing only a pair of CMOS transistors, with no additional resistors. Taking a small chip surface, in the planar integrated circuit technology, it is possible to use it for very high density integrated circuits.

One has to not that in any logical state, at least one of the two transistors, connected in series, is in the "OFF" state, acting as an open switch. As a result, the current drawn from the power supply, when no load is connected at the output, is very small. Therefore, the static dissipated power of a CMOS circuit is extremely small. However, the switching between states will result in a momentarily increase in the power consumption. The average power consumption in normal operation will be proportional to the frequency of transitions between different logic states.

Experimental Setup



The experimental setup includes on the same board a CMOS inverter, as well NOR, NAND, bi-directional switch and and inverter with 3-state output. On the board, four resistors that allow the application of high and low logic levels on circuit's inputs, as well as a LED that allows visualization of the output level are also provided. The board is powered from a single +10V power supply, using the banana jacks on the bottom-right side of the board. A DC milliammeter has to be inserted in series with the power supply, to monitor the current consumption in different operating regimes.

Experimental Measurements

CMOS Inverter

To start with, we will verify the truth table of the inverting circuit and we will measure the static power consumption.

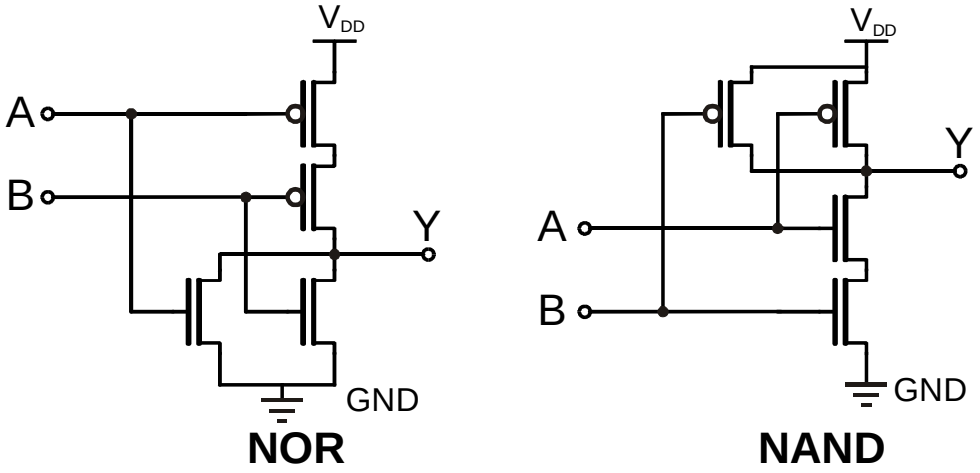
> Please connect in series with the power supply a DC milliammeter and adjust the power supply voltage to 10V. Connect the LED to the Y output, in order to be able to visualize its state. Apply to inverter's input Logic levels low (binary 0) and high (binary 1) using the pull-up and pull-down resistors and fill in the truth table below:

A	Y

Disconnect the LED from inverter's output and measure the supply current I_D. Verify that the current is negligible regardless of the logic state of the inverter circuit.

NOR and NAND Gates

Implementation of more complex logic functions like NOR or NAND is based on connecting several complementary transistors in particular configurations.



For the NOR circuit shown above, if on any of the inputs (A or B) we apply a high voltage level, at least one of the n-MOS transistors connected in parallel will be in the ON state, pulling down the output. Only when both inputs are pulled low, the p-MOS transistors connected in series will be in ON state, pulling the output high.

Connect the LED to the output Y of the NOR circuit and apply all combinations of low (0) and high (1) levels using the pull-down and pull-up resistors on circuit board. Fill in the truth table of the circuit:

A	B	Y

Analyzing the NAND circuit structure, shown above, we see that any of the inputs A or B pulled down (0) will bring at least one of the p-MOS transistors in the ON state, leading to a high level at the output. If both inputs are pulled up (1) both n-MOS transistors connected in series will be in ON state, pulling down (0) the output.

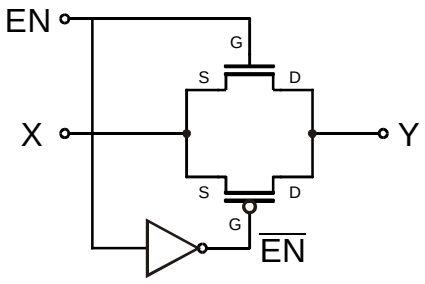
Connect the LED to the output Y of the NAND circuit and apply all combinations of low (0) and high (1) levels using the pull-down and pull-up resistors on board. Fill in the truth table of the circuit:

A	B	Y

Disconnect the LED and verify that the supply currrent is negligible, regardless of the logic state of the inverter circuit.

Bi-directional switch

The bi-directional switch is a circuit that is specific to (C)MOS technology. This type of circuit cannot be implemented using bipolar junction transistors, for instance. It consists of a pair of complementary transistors, with both sources and drains connected together to two input/outputs X and Y. On the gate of the n-type MOS, an ENABLE signal is applied, whereas on the gate of the p-MOS an inverted copy of the ENABLE signal is applied.



Bi-directional switch

Whenever a high voltage level (binary 1) is applied to the ENABLE (EN) input, the n-MOS transistor is in the ON state, as long as the difference between the gate and source voltage (between ENABLE and X) is greater than the threshold voltage V_T. The voltage level applied on the gate of the p-MOS transistor is at the same time low ($\overline{EN}$), such that the p-MOS transistor is in the ON state as well, as long as the difference between gate and source voltage exceed V_T. One can see that whenever the condition of a gate-source voltage greater than the threshold voltage is not met for one transistor, it is always met for the complementary transistor, such that at any time at least one transistor is in conduction (ON) state, for the entire range of input/output voltages, matching the power supply voltage (V_{SS}, V_{DD}). This is the reason for using a pair of complementary MOS transistors instead of a single n-MOS or p-MOS transistor. The drain-source circuits of the two transistors therefore behave as closed switches between X and Y. By applying a low voltage level (0) on the ENABLE switch, using a similar analysis we can see that both transistors are in the OFF state, acting as open switches between input and output.

The switch operates not only for digital signals on X and Y, having values close to V_{SS} or V_{DD}, but for any voltage level in between the power supply rails (V_{SS}, V_{DD}). Therefore the switch can be used with analog signals as well, being called **analog**

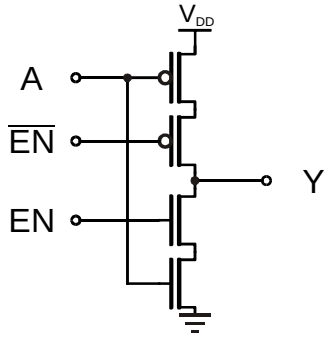
bi-directional switch, this circuit property making it widely used in analog circuitry as a solid-state switch or relay.

Please connect an ohmmeter between X and Y points of the bi-directional switch. Use the CMOS inverter circuit for obtaining an inverted version of the EN signal and connect it to the gate of the p-MOS transistor, as in the schematics above. Apply low and high voltage levels on the EN input, while noting the impedance change of the switch. Fill in the measurement results in the table below:

E N	Z
0	
1	

Three-state output circuits

The configuration of the digital circuits we have analyzed so far, using either bipolar junction transistor or field-effect transistors, did not allow connecting in parallel the outputs of several circuits, as they would interfere with each other. Having the ability to connect outputs of multiple circuits in parallel and selectively enable them, one at a time, would greatly simplify the construction of complex circuits. This so called "BUS" configuration is heavily used in digital and microprocessor circuitry. By modifying the inverter circuit, like in the figure below, by inserting one transistor of each type in series with the existing ones and connecting them to $EN / \overline{EN}$ signals, we obtain a circuit whose output can be either active, in the high (1) or low (0) states, or inactive, in a high-impedance state (Hi-Z). This is behind circuit's naming of "tri-state". Using a similar reasoning path as for the bi-directional switch, we see that whenever the EN signal is high, the output Y is connected to the two transistors in the original inverter schematics, whereas for EN signal low, the output Y is disconnected.



3-state inverter

Use the CMOS inverter circuit for obtaining an inverted version of the EN signal and connect it to the gate of the p-MOS transistor. Connect the LED at the output of the circuit. Apply a high voltage level on the EN input and verify the operation of the circuit as an inverter. Apply a low voltage level on the EN input and check that regardless of the logic level on the A input, the LED is off. To verify that the non-illuminated LED state does not correspond to a zero

output level, but to a Hi-Z level, disconnect the LED and connect an ohmmeter between output and ground. Write down the impedance reading.
CAUTION: ***connect the ohmmeter while the EN input is low (0), or else an active high output can damage the measurement circuitry of the ohmmeter.***

CMOS power dissipation

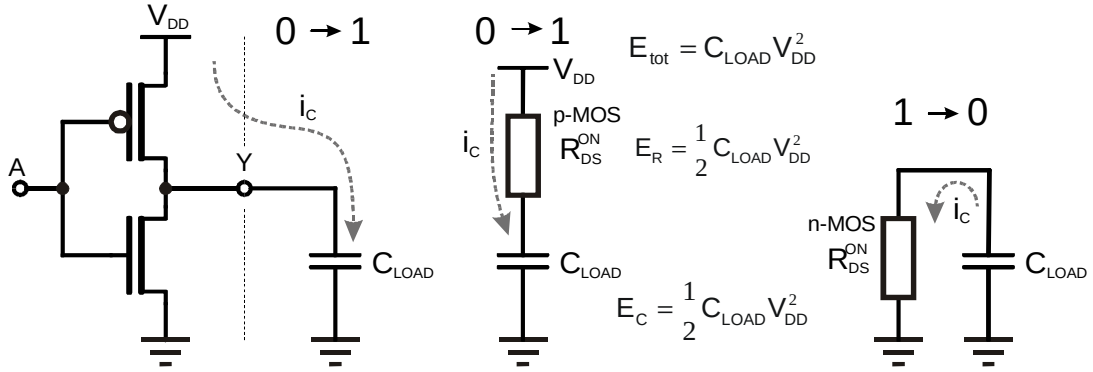
As mentioned in the beginning, the static power dissipated by the CMOS circuits is extremely small. However, some current is drawn momentarily from the power supply whenever the CMOS circuits change their state. We will illustrate this on the simplest CMOS circuit, the inverter. In the static regime, with no load connected at the output, at least one of the n-MOS or p-MOS transistors is in the OFF state, such that there is negligible current drawn from the power supply and correspondingly low dissipated power ($P = I_D V_{DD}$).

Disconnect the LED from the output of any gate and measure the current I_D drawn from the power supply by all CMOS circuits on the board. Calculate the dissipated power using the formula:

$$P = I_D V_{DD}$$

By connecting the inputs of various logic circuits to logic levels 0 or 1, check that the dissipated power remains very small, regardless of the input/output states.

Even for very complex digital circuits, that may contain millions of logic gates, the dissipated power in static regime can be very small. However, when the circuits are in normal operating regime, by changing their states at frequencies of the order of magnitude of MHz or GHz, the power required for charging and discharging various capacitances in the circuitry starts to play a significant role.
To illustrate that, we have represented in the figure below the process of charging and discharging a capacitor. In an actual circuit, the capacitor can represent for instance the equivalent gate-source and gate-drain capacitances of another gate that is being driven (C_{LOAD}).



Starting with a discharged capacitor and a zero output level, whenever the output switches to the high level, the p-MOS drain-source circuit will have a low ON resistance, R_{DS}^{ON}. The load capacitor C_{LOAD} will be connected through R_{DS}^{ON} to the power supply voltage V_{DD} and the current drawn from the power supply, i_c, will charge it following an exponential law. The energy stored in the capacitor, when fully charged, will be:

$$E_C = \frac{1}{2} C_{LOAD} V_{DD}^2$$

The resistor in series with it, R_{DS}^{ON}, will dissipate an equivalent amount of Joule energy E_R, regardless of its resistance value:

$$E_R = \frac{1}{2} C_{LOAD} V_{DD}^2$$

Therefore, the amount of energy required to make a 0->1 transition is:

$$E_{tot} = C_{LOAD} V_{DD}^2$$

For the opposite 1->0 transition, the p-MOS transistor goes into the OFF state, while the n-MOS one goes into the ON state. The previously charged capacitor will discharge to ground through the R_{DS}^{ON} of the n-MOS capacitor. The entire energy stored on the capacitor will be dissipated on the R_{DS}^{ON} resistor, this process taking place without any additional power drawn from the power supply.
For a circuit that operates at a frequency f, the total power P_{tot} dissipated by n CMOS gates will be:

$$P_{tot} = n \cdot C_{LOAD} \cdot V_{DD}^2 \cdot f$$

> Please connect at the input of the inverter circuit a signal generator and change the frequency in the 0-10MHz range, while measuring the I_d current drawn from the power supply. Please make sure that you configure the signal generator to provide at the output a square waveform with a peak-to-peak amplitude of 10 V and an offset of 5 V, such that the voltage swing will be between 0 and V_{DD} (+10 V). Use an oscilloscope to verify the waveform at the inverter's input. Measure I_d at different f values, calculate the dissipated power P and plot it as a function of f, using a linear scale. Verify that the power drawn from the power supply is approximately linear.

The dissipated power in the dynamic operation regime is not entirely due to the charging and discharging of various capacitances in the circuit. Another component refers to simultaneous opening of both transistors while making a transition from one state to the other. For a short duration during a transition, the transistors will short-circuit each other. This will happen in the interval where the input voltage will exceed the gate threshold voltage of the n-MOS transistor, but will not be high enough to switch the p-MOS transistor to the OFF state. We will illustrate this phenomenon by intentionally applying a voltage level at the input in this region, while measuring the supply current I_D.

To obtain a voltage that is about half of the supply voltage V_{DD}, connect together one pull-up with a pull-down resistor (located on the bottom-left side of the circuit board). A resistive divider will be formed, providing a $V_{DD}/2$ (+5 V) two of the resistors. Select the 1 A ammeter range and briefly connect (<1 s) the $V_{DD}/2$ voltage to the input of the inverter, while measuring the peak current drawn from the power supply.

Caution: ***do not apply*** $V_{DD}/2$ ***on any input for more than 1-2 seconds, as this will damage the transistors through overheating. Do not use a DC current scale lower than 1 A, as this may damage the ammeter.***